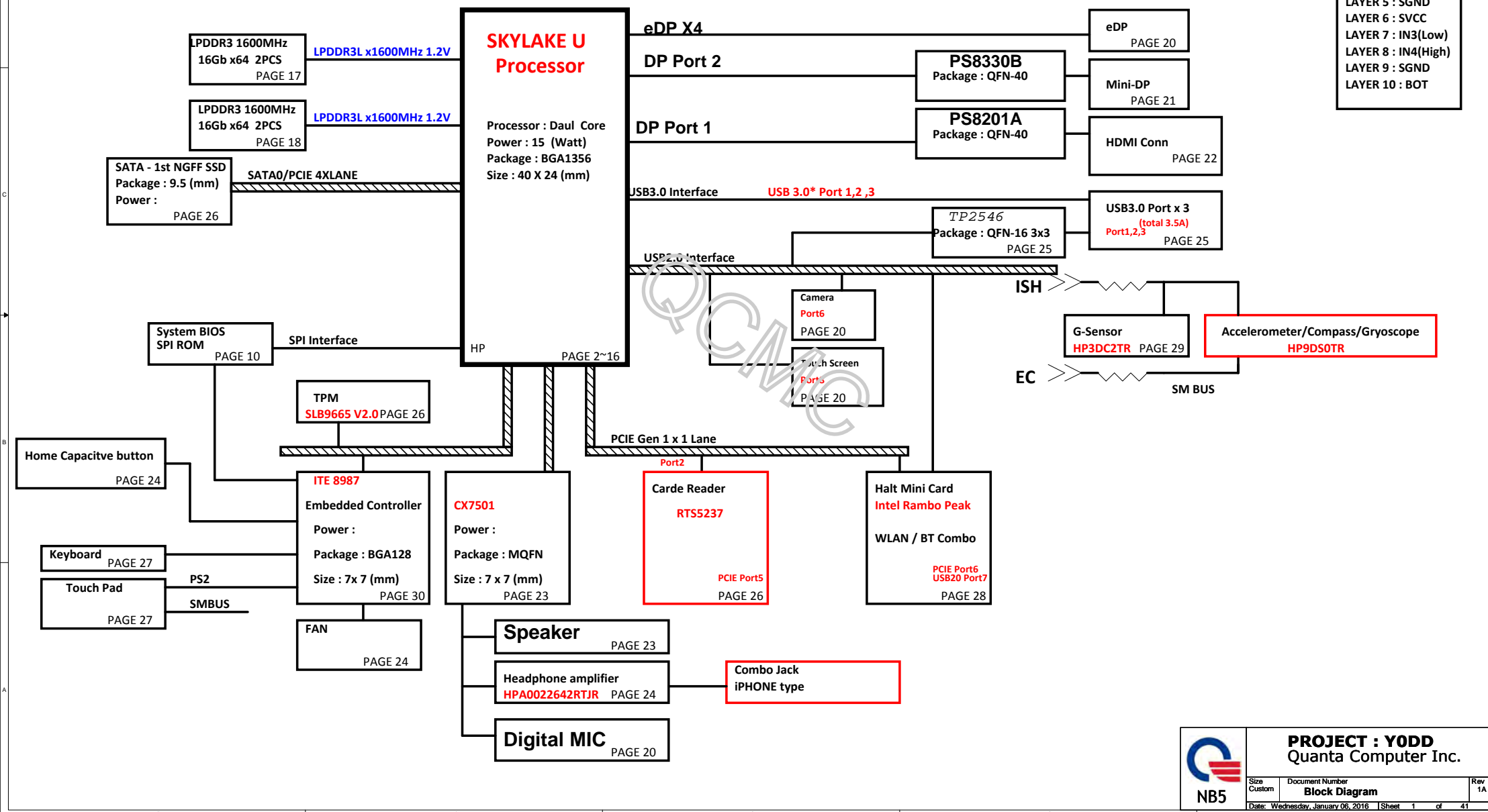


Pike Intel SKYLAKE ULT Platform Block Diagram

PCB 10L STACK UP

LAYER 1 : TOP
 LAYER 2 : SGND
 LAYER 3 : IN1(High)
 LAYER 4 : IN2(High)
 LAYER 5 : SGND
 LAYER 6 : SVCC
 LAYER 7 : IN3(Low)
 LAYER 8 : IN4(High)
 LAYER 9 : SGND
 LAYER 10 : BOT



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Block Diagram		
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+3V 4,10,11,12,13,14,15,20,22,23,26,27,29,30,31,37,38
+1.0V 4,6,30,36
+VCCSTPLL 5,6,9,36,38
+VCCIO 6,16,36

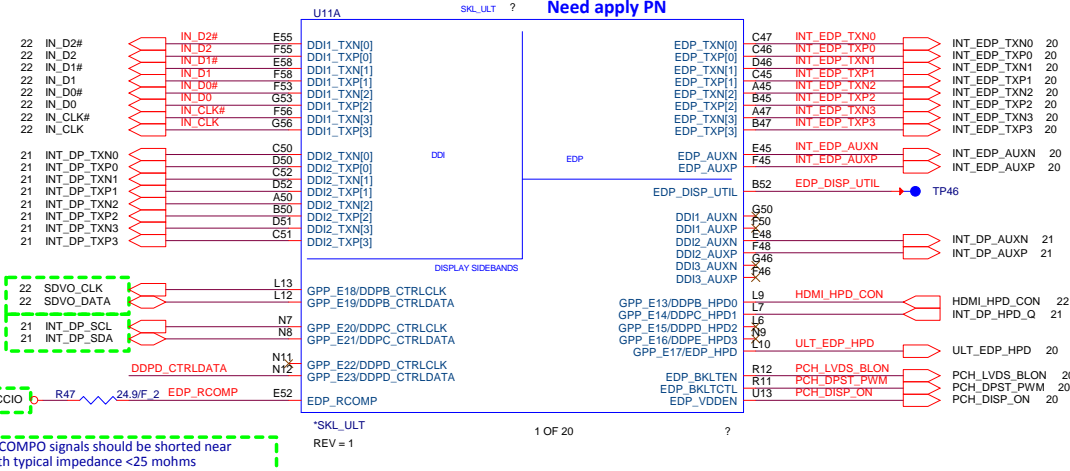
HDMI

INT_DP_SCL R245 2.2K 2
INT_DP_SDA R246 2.2K 2

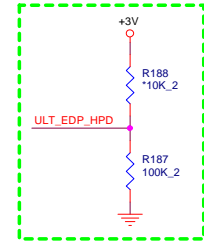
DDPB_CTRLDATA/ GPP_E19
Display Port B Detected
This signal has a weak internal pull-down.
0 = Port B is not detected.
1 = Port B is detected.

This signal has a weak internal pull-down.
0 = Port C and D is not detected.
1 = Port C and D is detected.

DDPD_CTRLDATA R51 10K 2

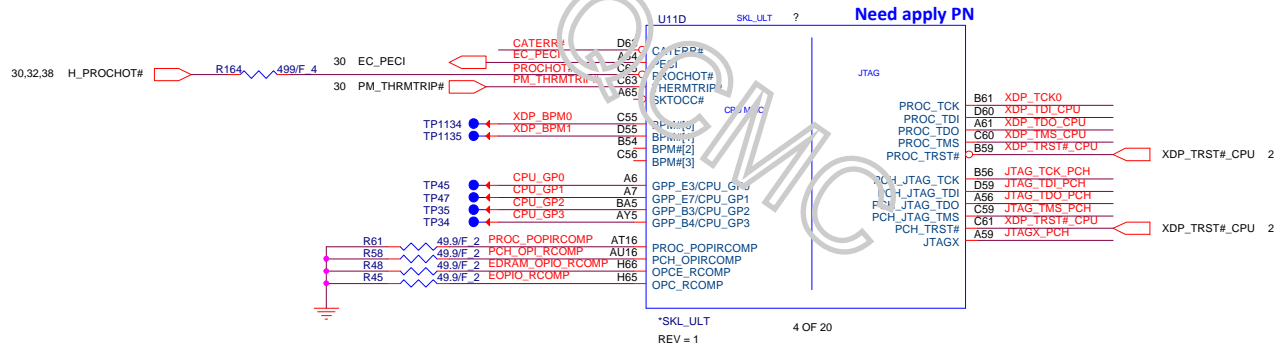
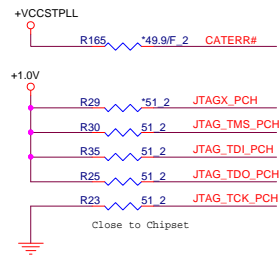


Reserve EDP_HPD opposites circuit!



Mini-DP

eDP_COMPIO and ICOMPIO signals should be shorted near balls and routed with typical impedance <25 mohms



Close to EC

PM_THRMTRIP# R213 1K 4

Processor pull-up (CPU)
TO BE REPLACED WITH 1K OHMS FOR SKL.
470 OHM IS FOR I/P

PLACE NEAR CPU

XDP_TMS_CPU R36 51 2
XDP_TDI_CPU R31 51 2
XDP_TDO_CPU R28 51 2

H_PROCHOT# R142 1K 2
XDP_TCK0 R177 51 2
XDP_TRST#_CPU R27 51 2



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SkyLake ULT Processor (DDR3L)



+1.2VSUS 6,17,18,34,36

Need apply PN

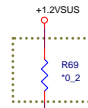
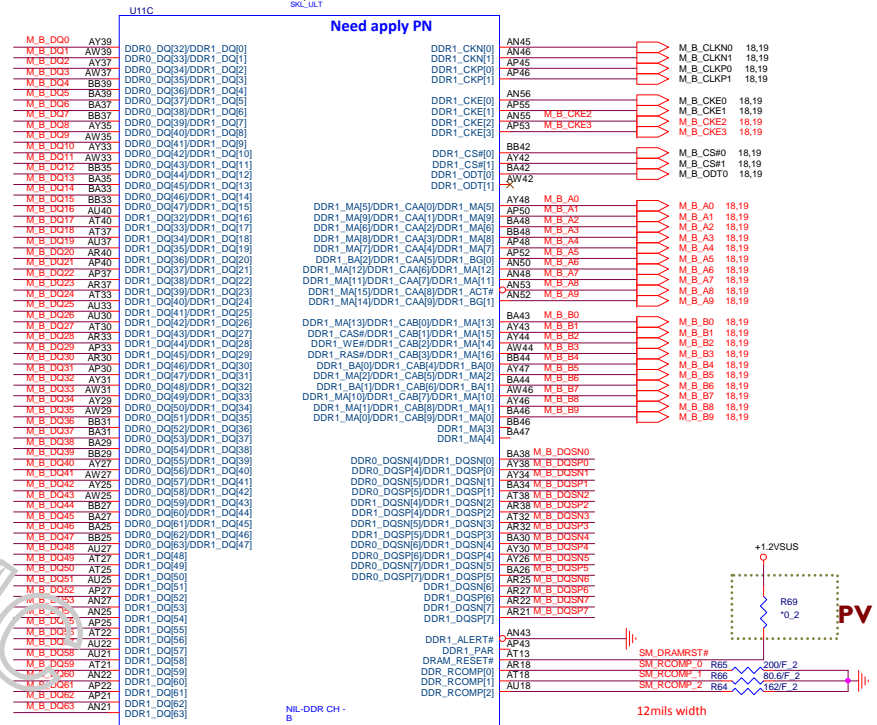
*SKL_ULT
REV = 1

2 OF 20

20mils width

Place near CPU

2

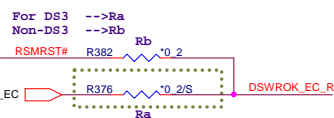
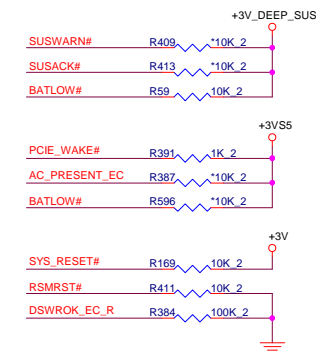
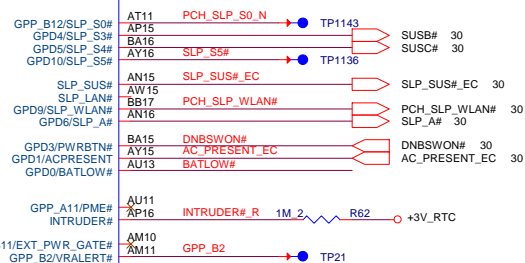
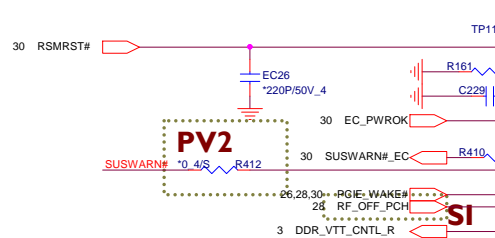


12mils width

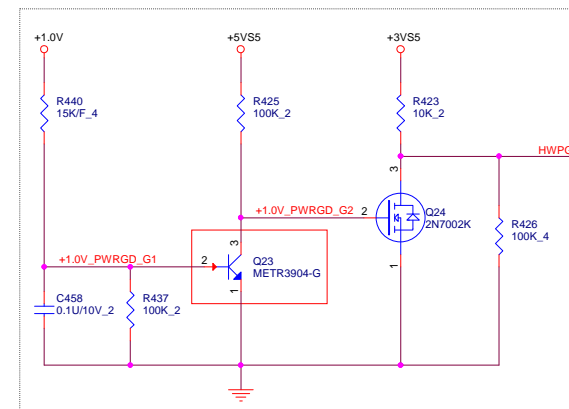
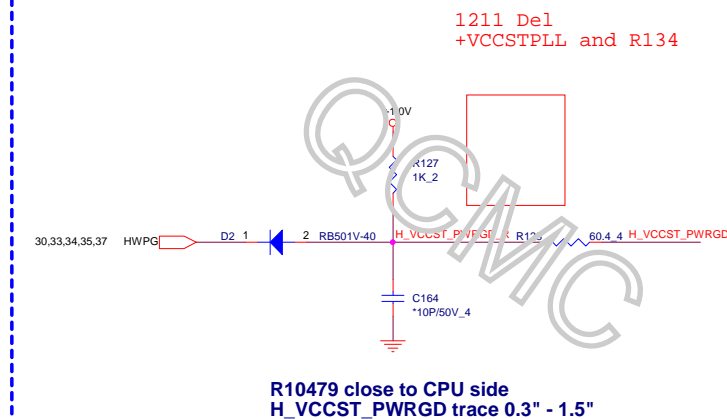
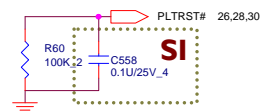


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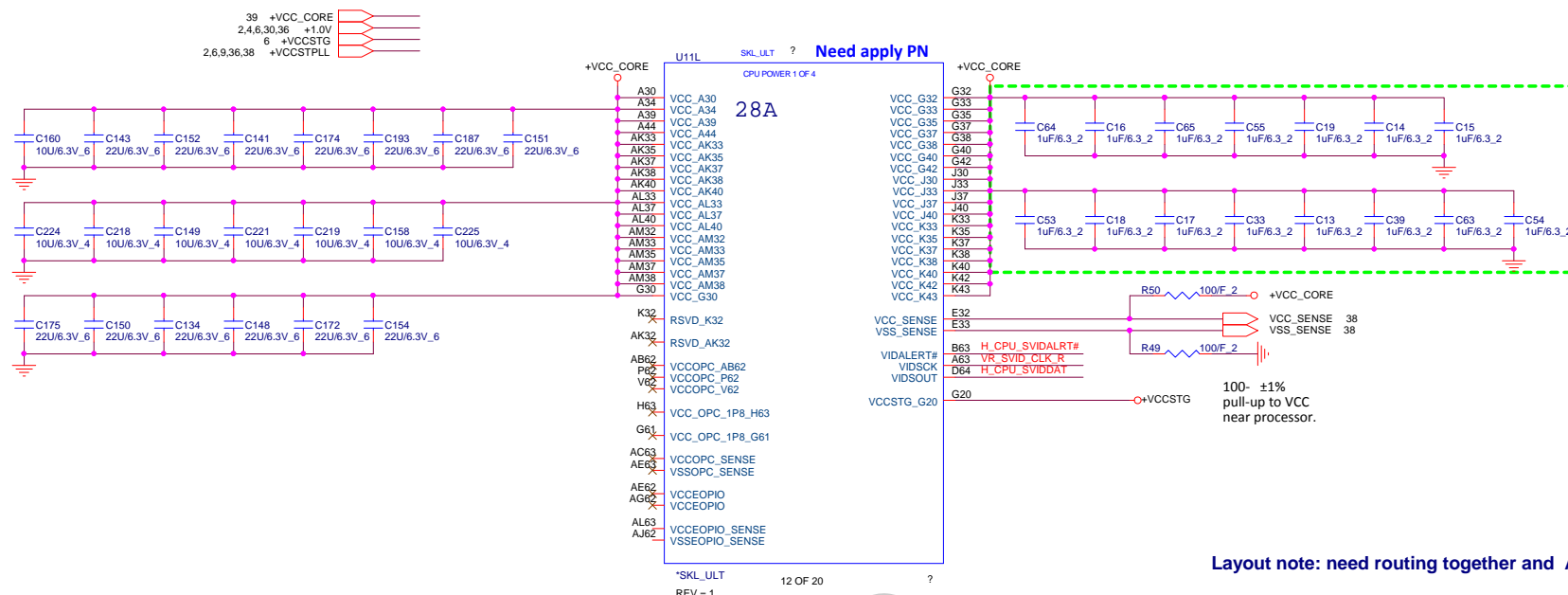


Check Q2010 Rise/Fall time less than 100ns

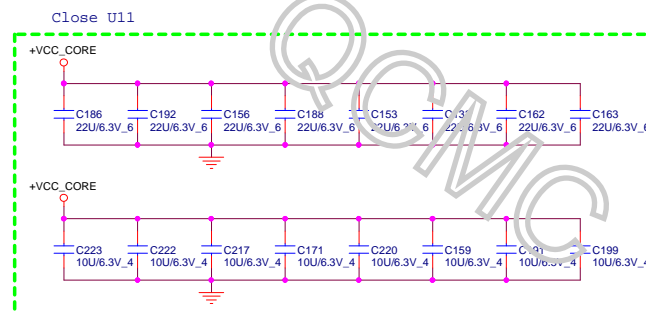


```
1110 Add Citecuit for +1.0V Power Good
```

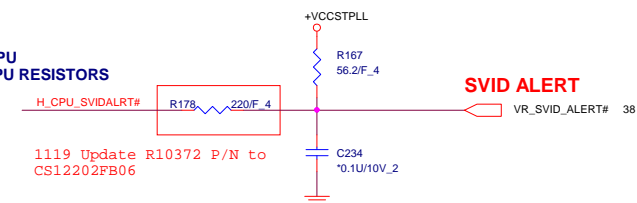
1118 Change Change Q7062 P/N from BA051440000 to
BA039040020, Del D7002,D7003, R10526, R10527



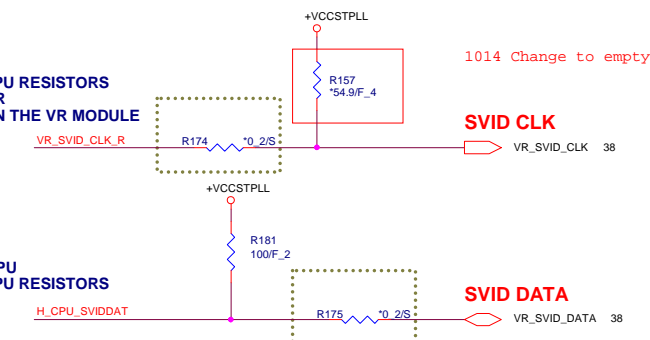
Layout note: need routing together and ALERT need between CLK and DATA.



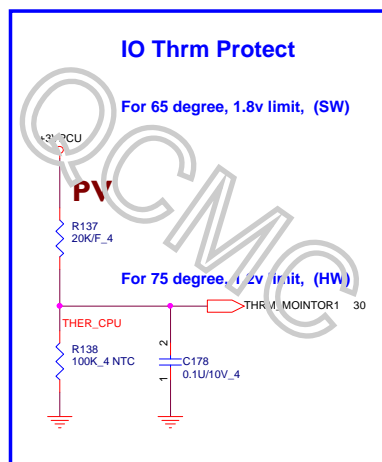
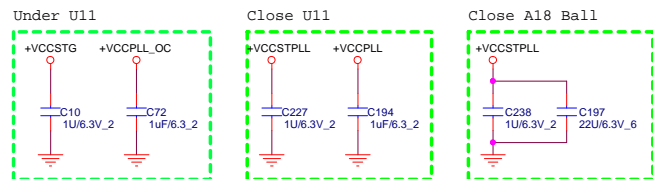
CLOSE TO CPU
PLACE THE PU RESISTORS



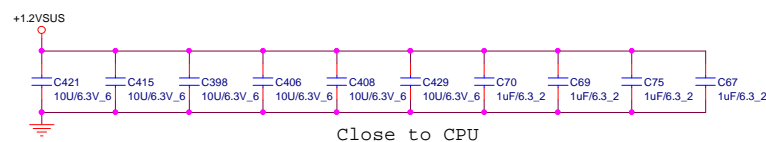
PLACE THE PU RESISTORS
CLOSE TO VR
PULL UP IS IN THE VR MODULE

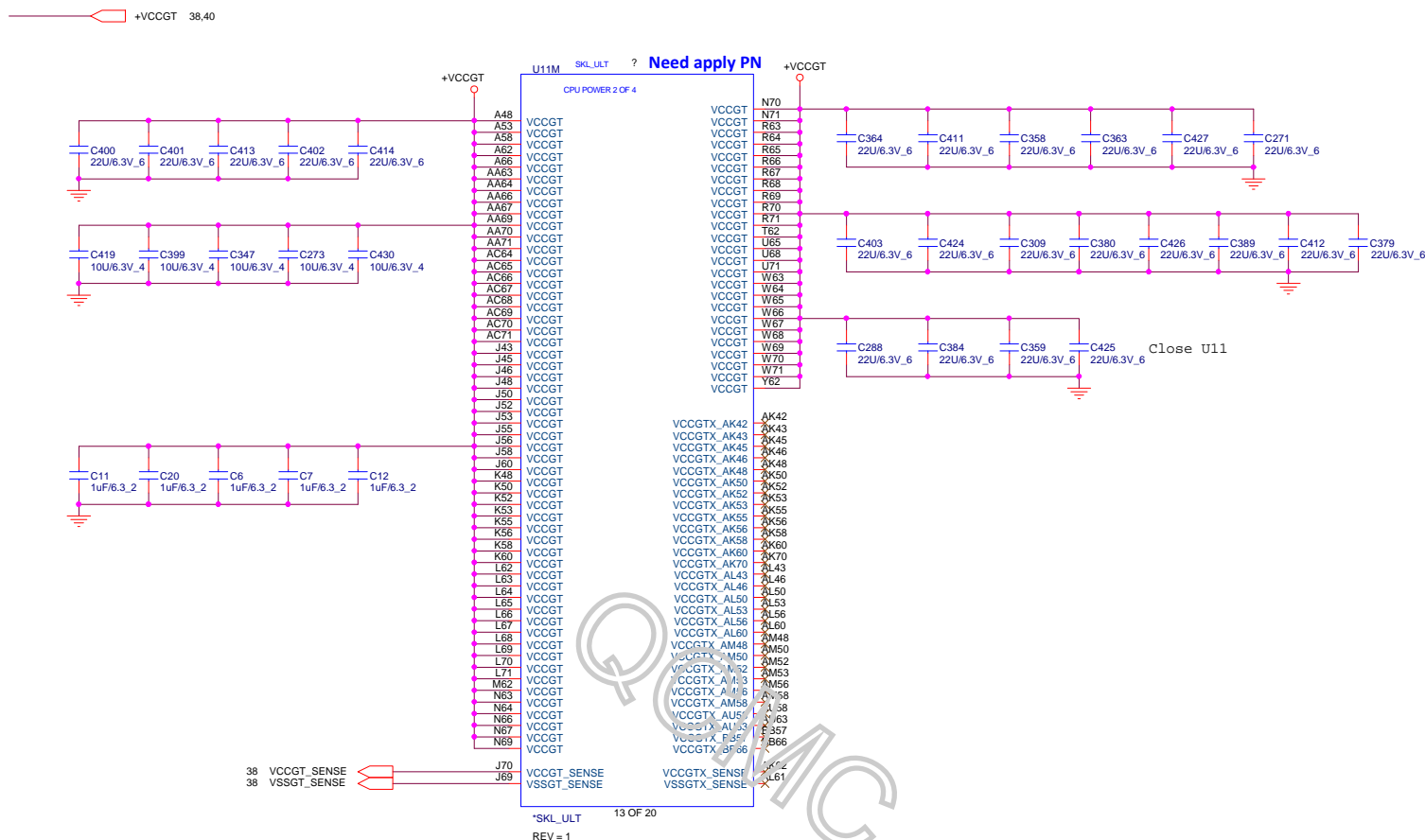


Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTx}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCEOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

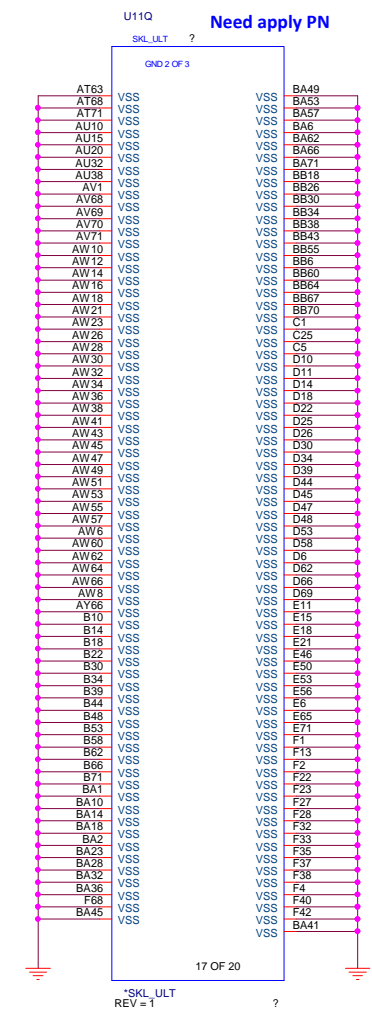
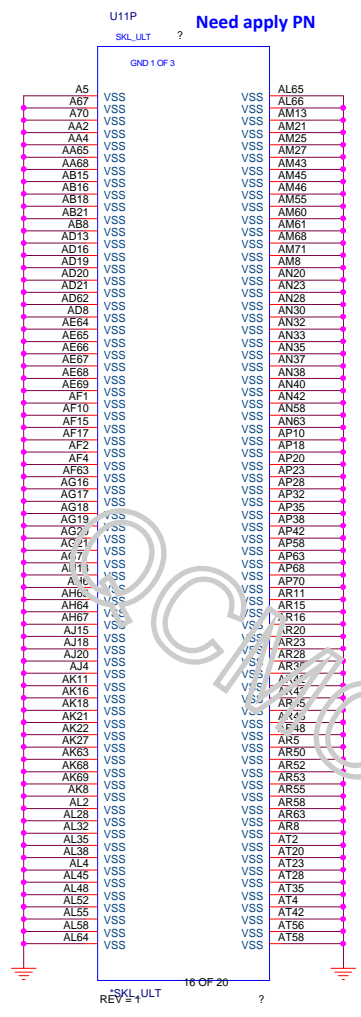
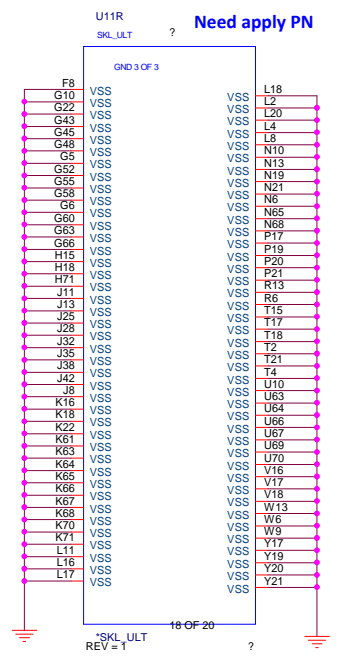


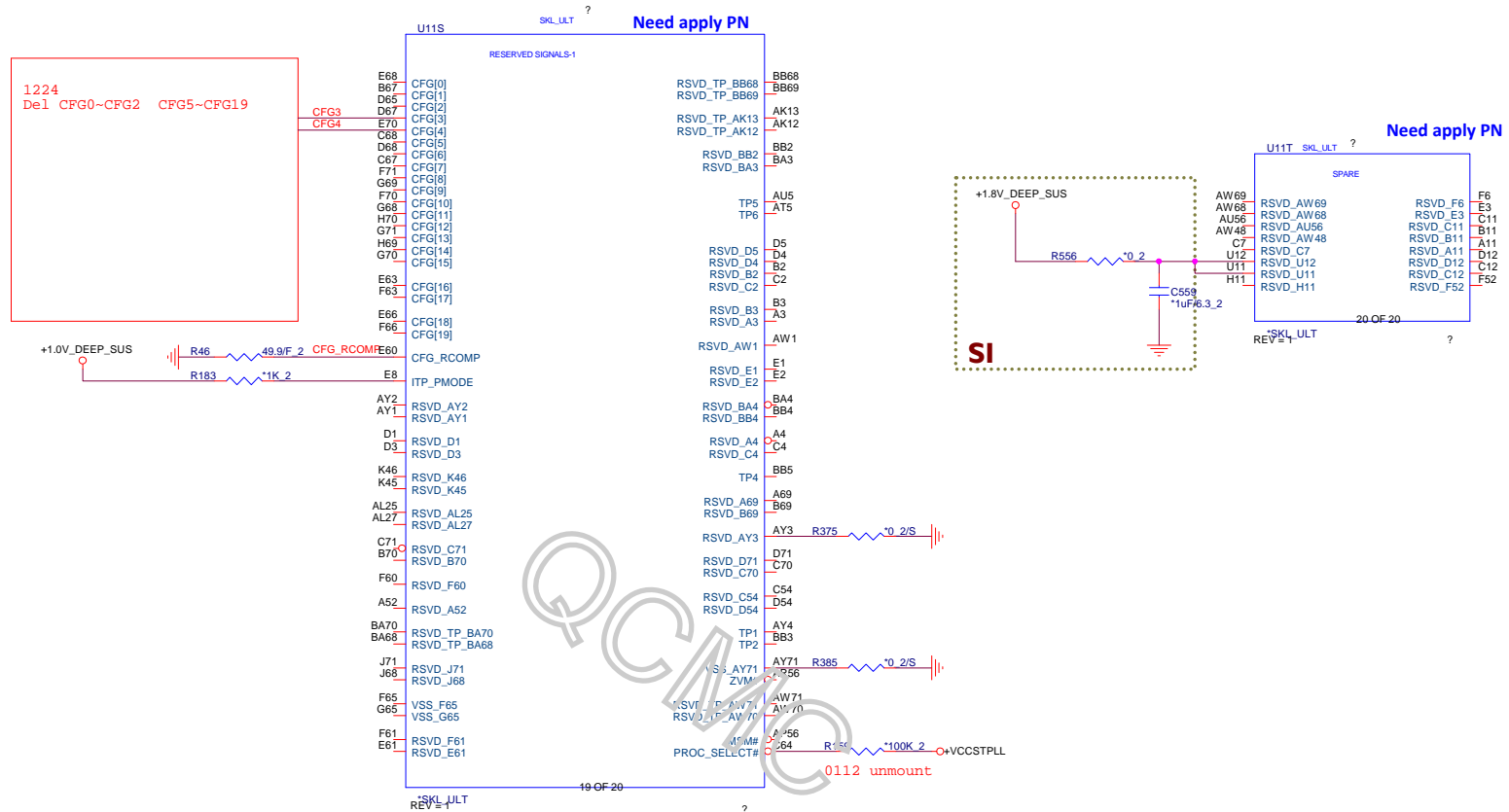
Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCEOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed





Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_IP8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCEOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed



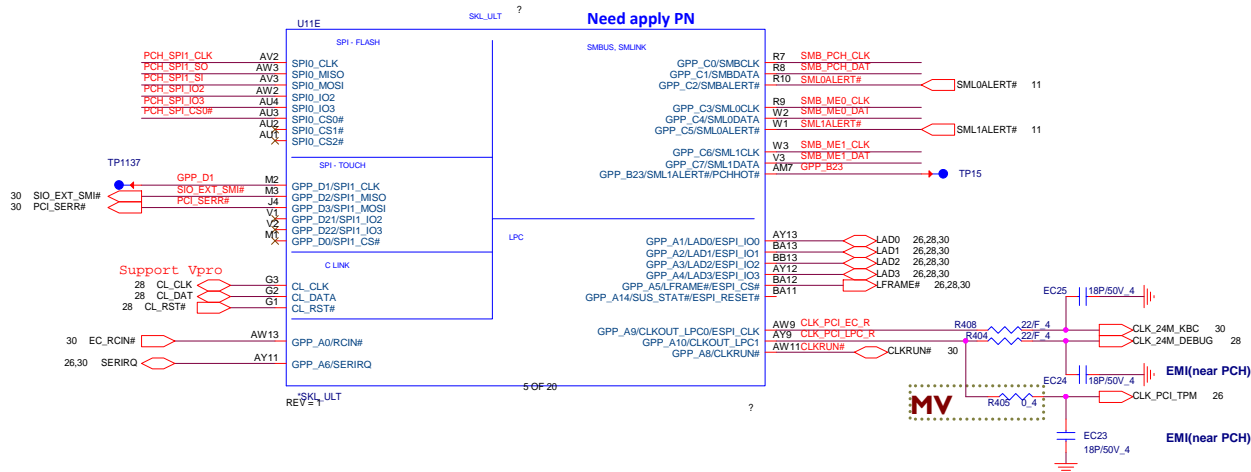


Processor Strapping

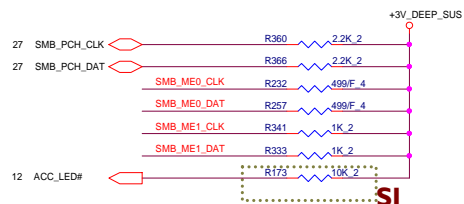
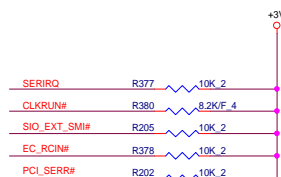
The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physical Debug Enable) DFX_Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R143 49.9K 2
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R42 1K 2

+3V_DEEP_SUS 4,11,12,14,15,27
+3V 2,4,11,12,13,14,15,20,22,23,26,27,29,30,31,37,38
+5V 22,23,24,27,37
+10V 2,4,6,30,36
+3VSS 4,15,22,28,30,31,33,35,36,37



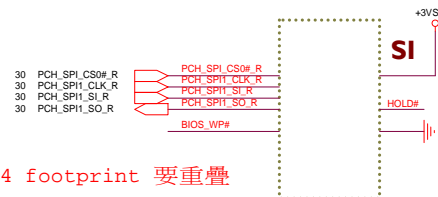
GPIO Pull UP



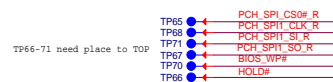
PCH SPI ROM(CLG)

Vendor	Size	P/N
EON	8MB	AKE3EZN0Q01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFN0805S023

4M SPI ROM Socket

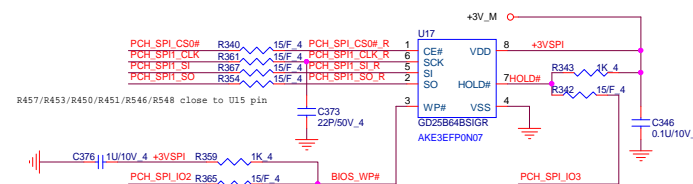


U23&U24 footprint 要重疊



PCH SPI ROM(CLG)

15 +3V_M



SMBus/Pull-up(CLG)

1230
Change net name from SMB_RUN_CLK to SMB_PCH_CLK
Change net name from SMB_RUN_DAT to SMB_PCH_DAT

Touch Pad
XDP

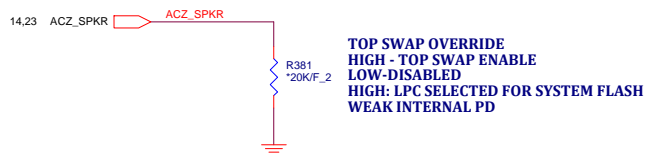


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Functional Strap Definitions

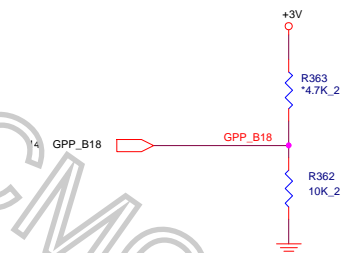
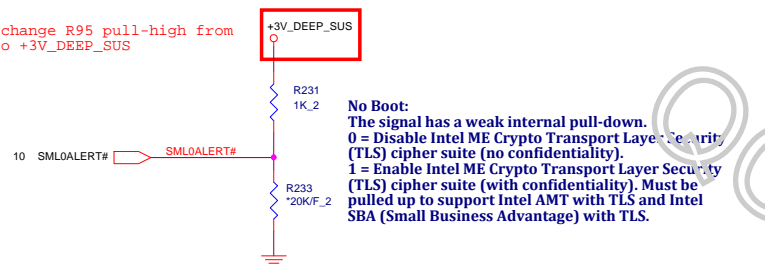
DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET



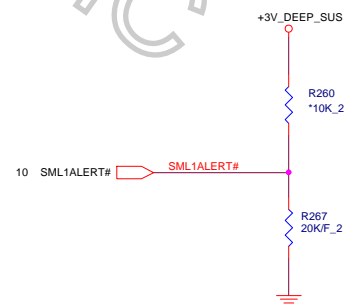
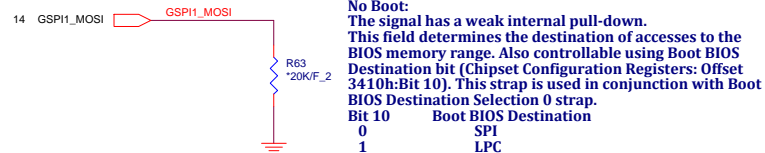
No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.



1212 change R95 pull-high from +3V to +3V_DEEP_SUS

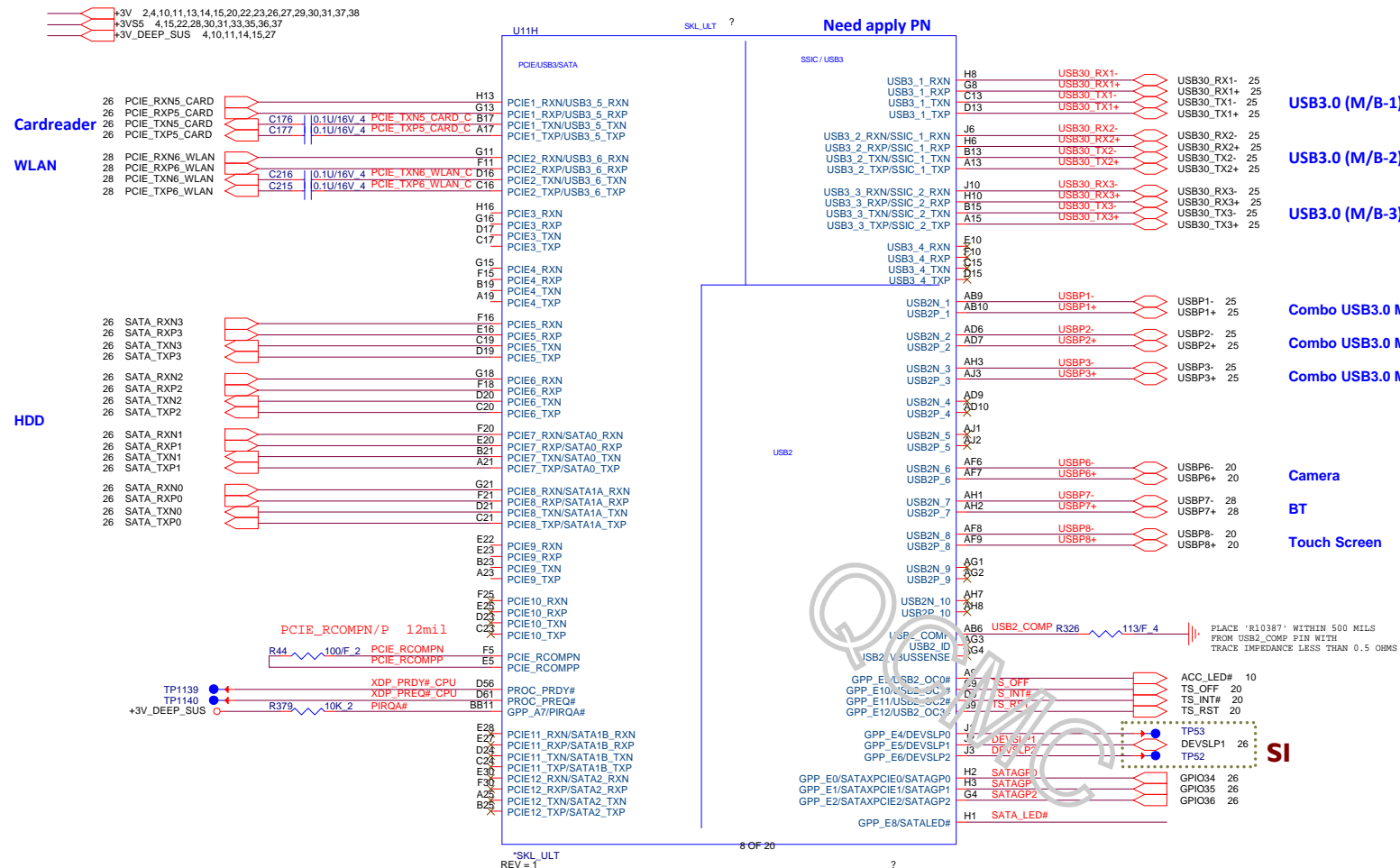


No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.



No Boot:
The signal has a weak internal pull-down.
0 = LPC is selected for EC.
1 = eSPI is selected for EC.

Need apply PN



PCI-E Port Mapping Table

PCI-E Port	Function	CLK RQ Port	Function
Port1	CardReader	Port0	Un-used
Port2	WLAN	Port1	CardReader
Port3	Un-used	Port2	WLAN
Port4	Un-used	Port3	Un-used
Port5	SSD	Port4	Un-used
Port6	SSD	Port5	SSD
Port7	SSD		
Port8	SSD		
Port9	Un-used		
Port10	Un-used		

USB3.0 Port Mapping Table

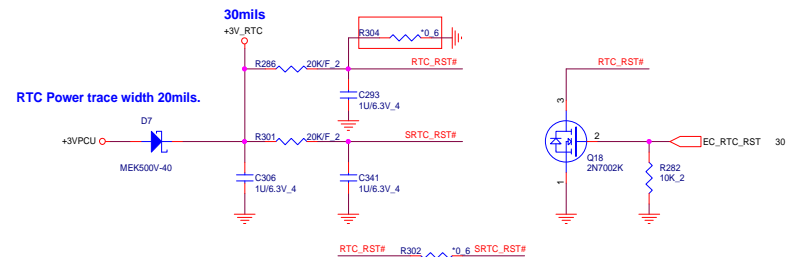
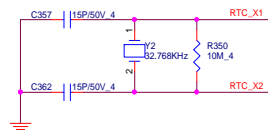
USB3.0	Function
PORT-1	USB3.0 MB-1
PORT-2	USB3.0 MB-2
PORT-3	USB3.0 MB-3
PORT-4	NC

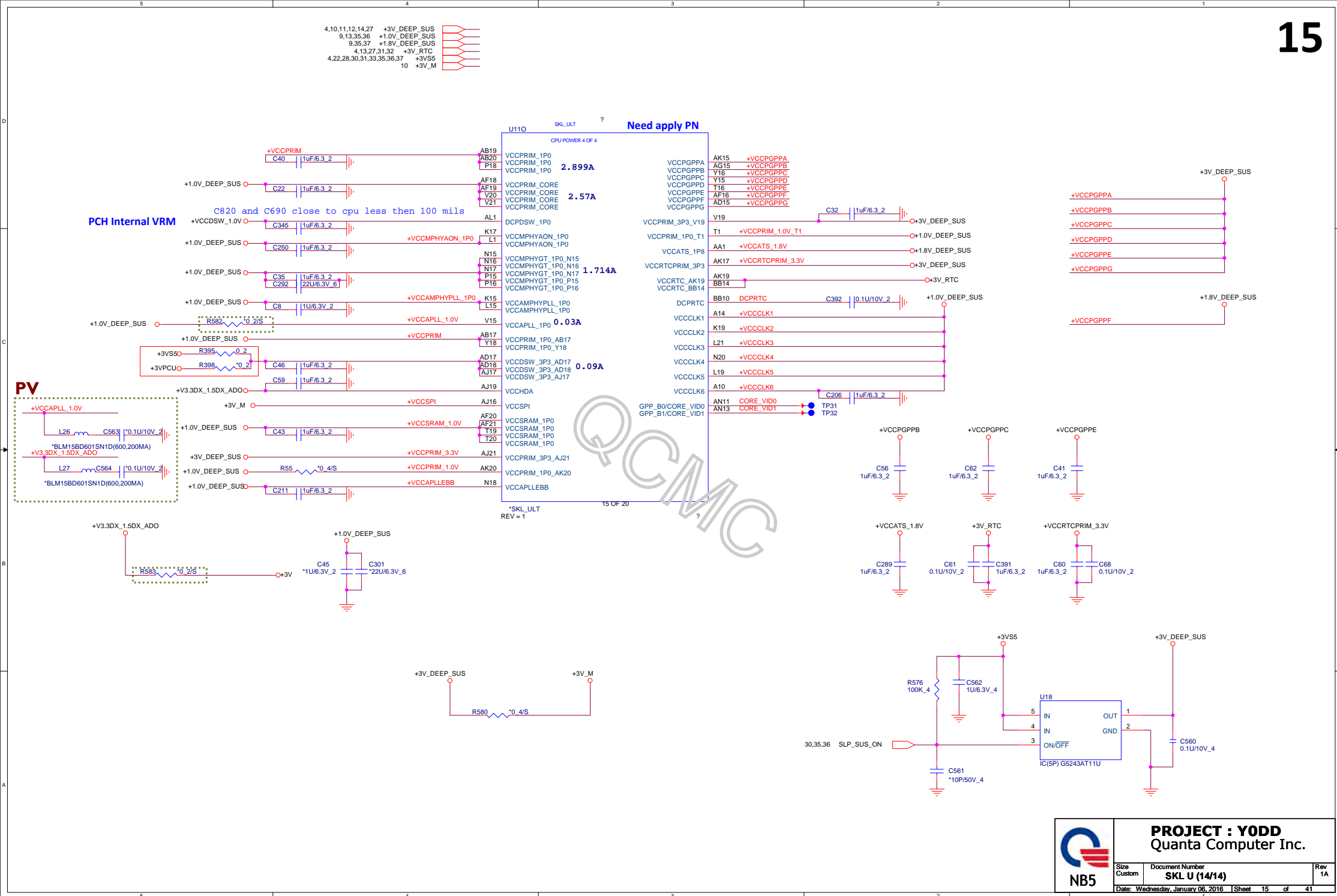
USB2.0 Port Mapping Table

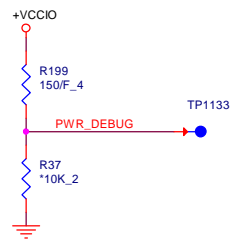
USB2.0	Function
PORT-1	USB3.0 MB-1
PORT-2	USB3.0 MB-2
PORT-3	USB3.0 MB-3
PORT-4	Sensor Hub
PORT-5	NC
PORT-6	Camera
PORT-7	WLAN
PORT-8	Touch Screen
PORT-9	NC
PORT-10	NC



 +3V_RTC 4,15,27,31,32
+3VPCU 6,15,27,28,30,31,32,33

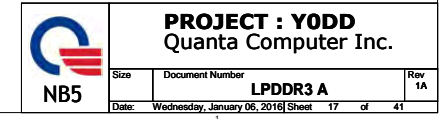




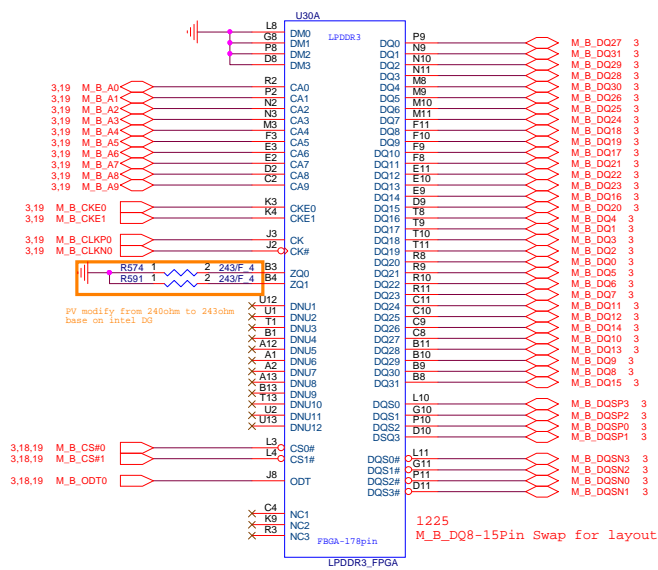


QCMC

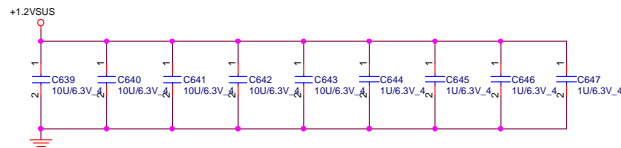
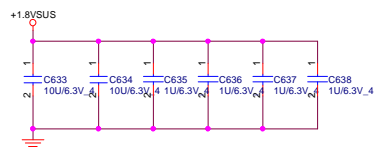
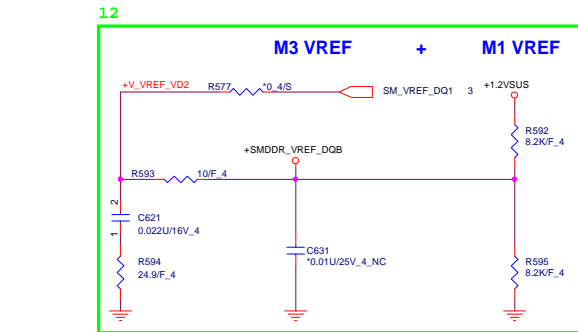
bit:32-63



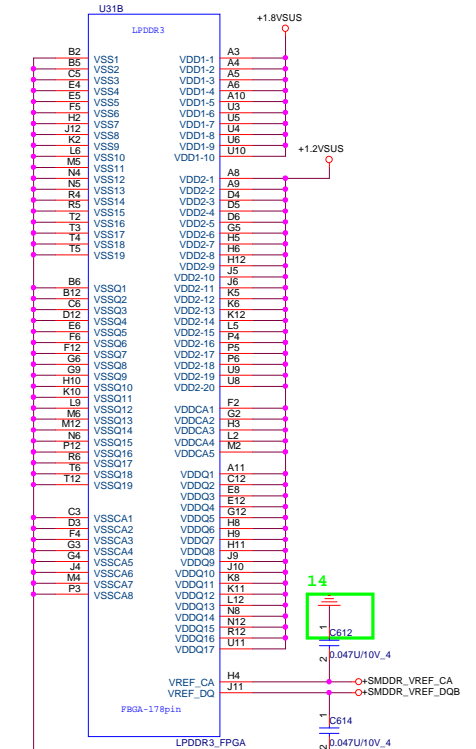
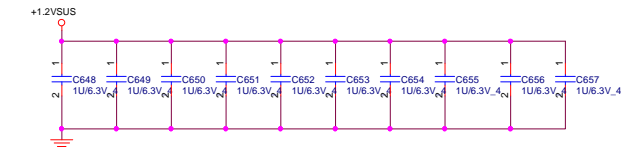
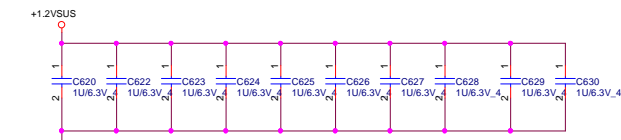
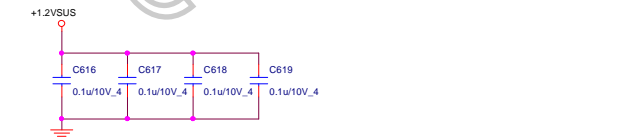
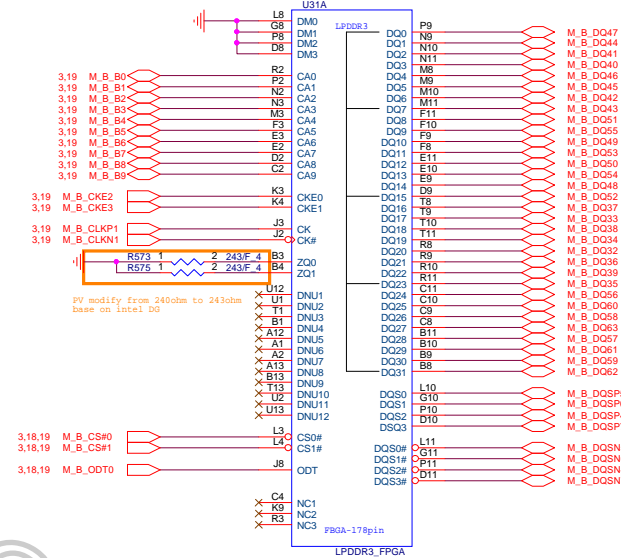
bit:0-31

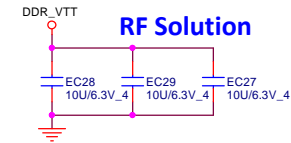
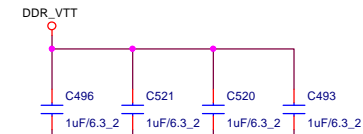
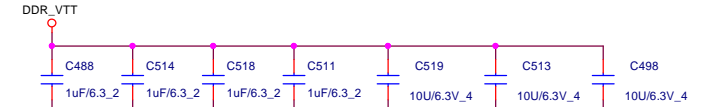
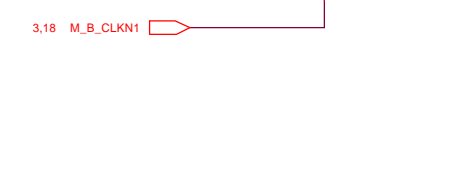
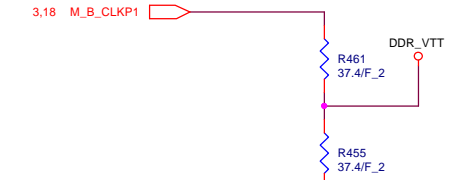
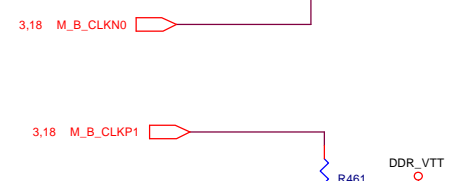
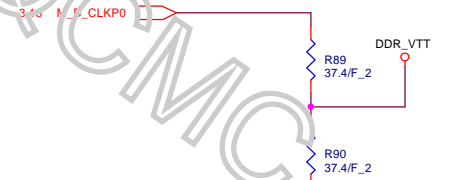
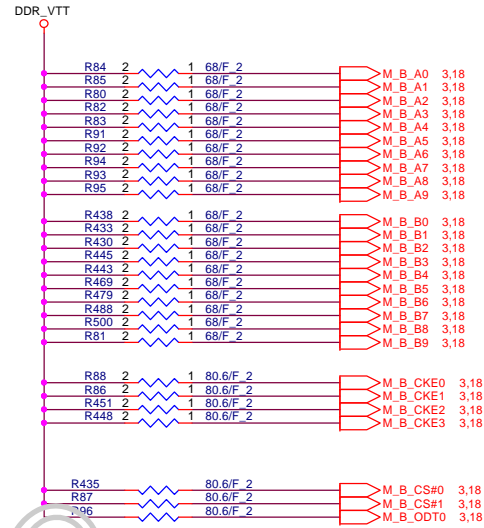
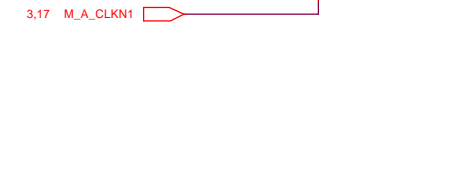
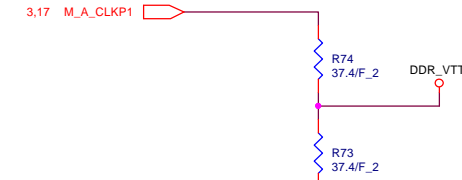
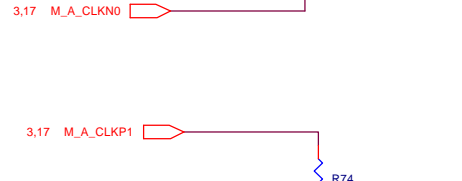
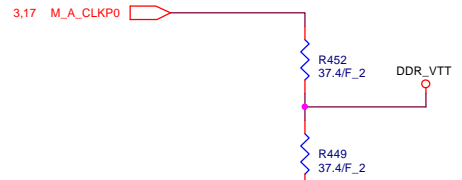
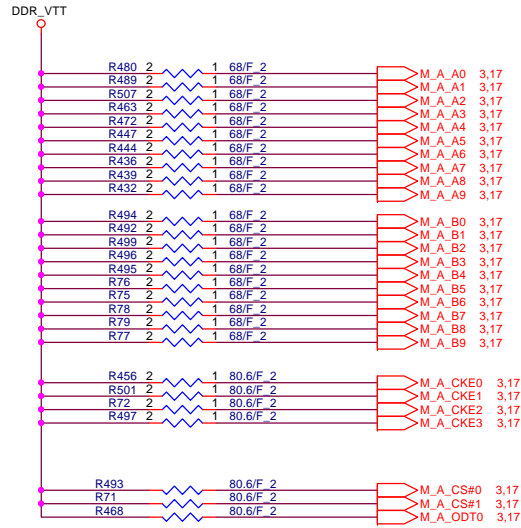


1225
M_B_DQ8-15Pin Swap for layout



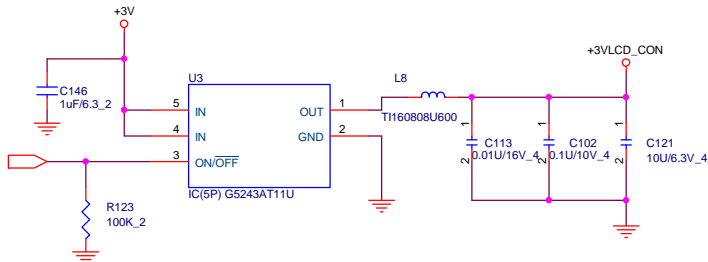
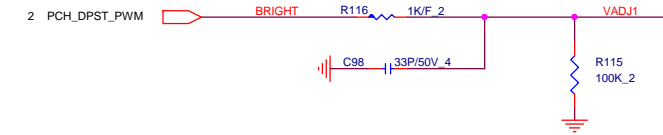
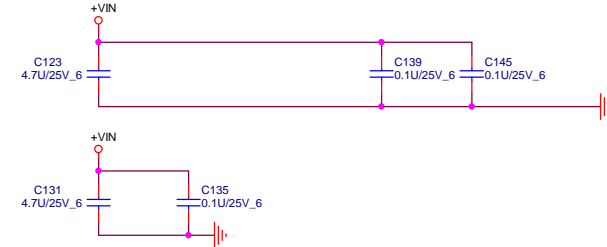
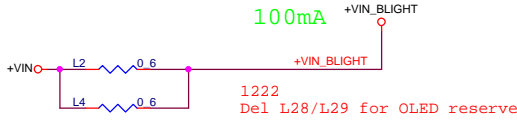
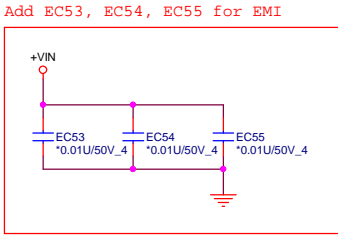
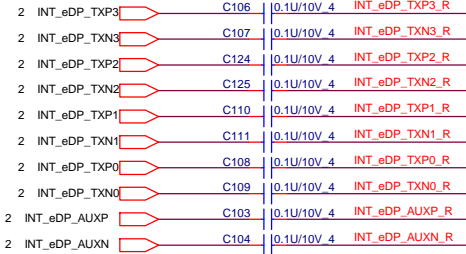
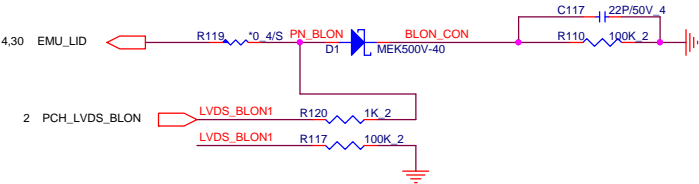
bit:32-63



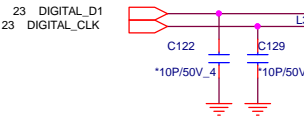


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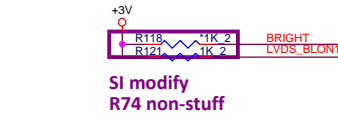
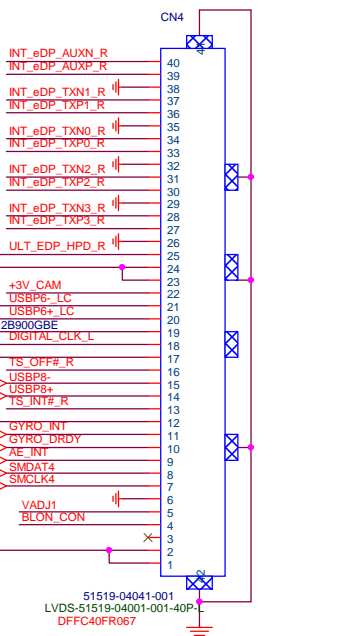
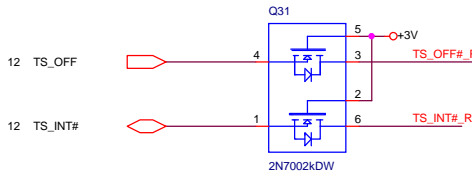
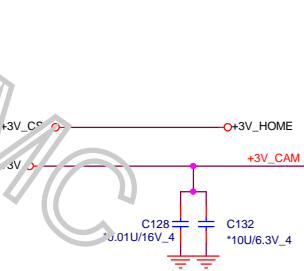
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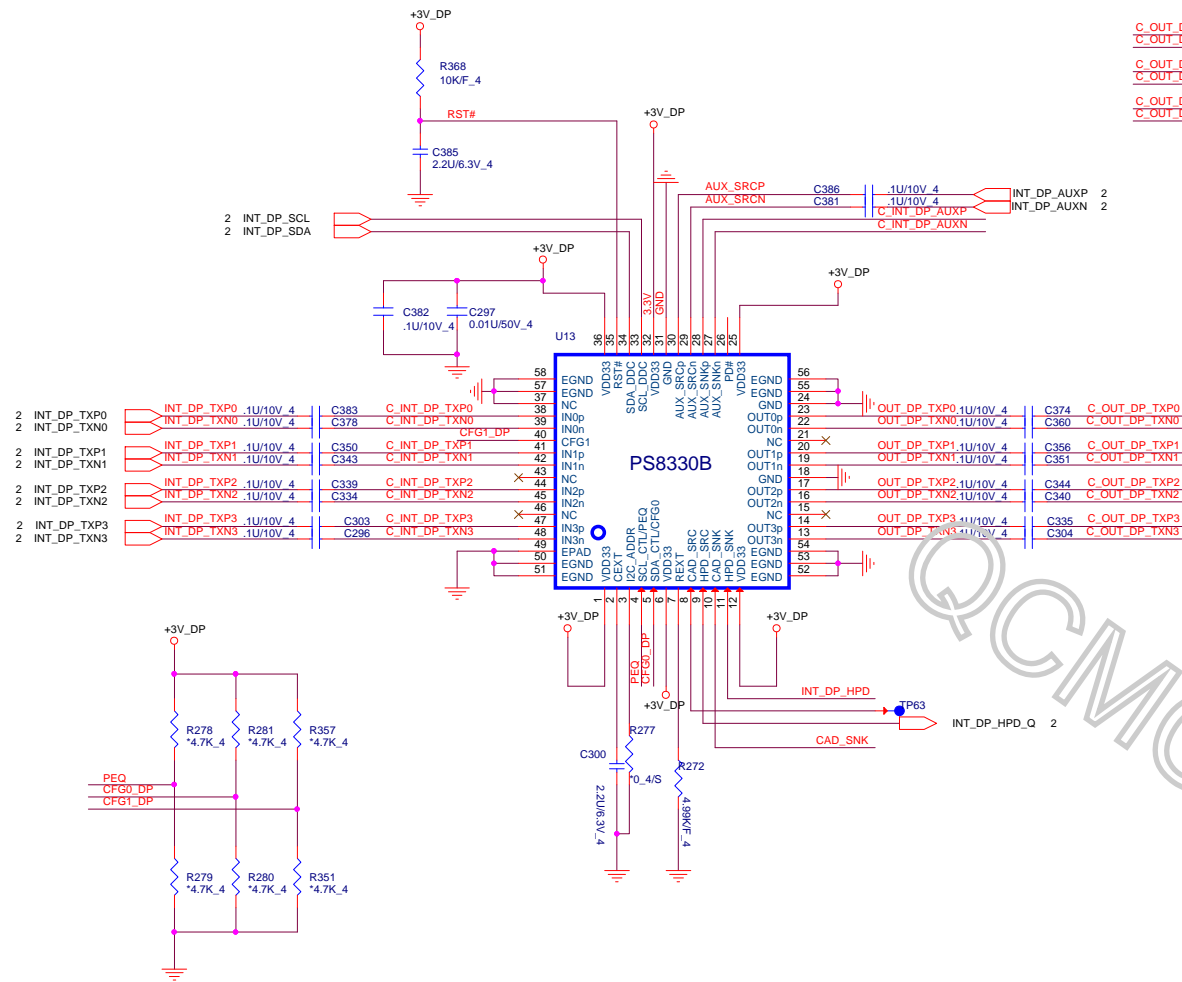
1225 L6 Pin Swap for layout



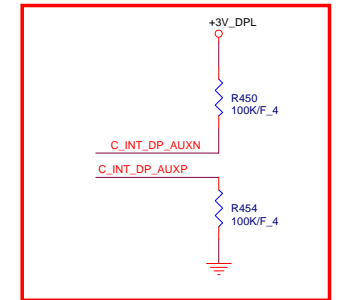
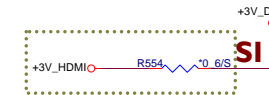
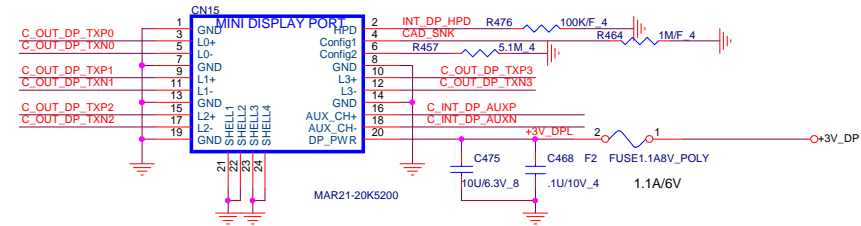
1222 Del C112/C101 for EMI reserve



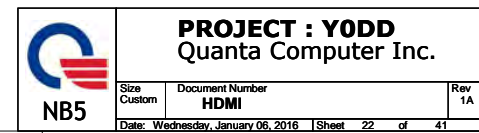
+5V 22,23,24,27,37
+3V 2,4,10,11,12,13,14,15,20,22,23,26,27,29,30,31,37,38

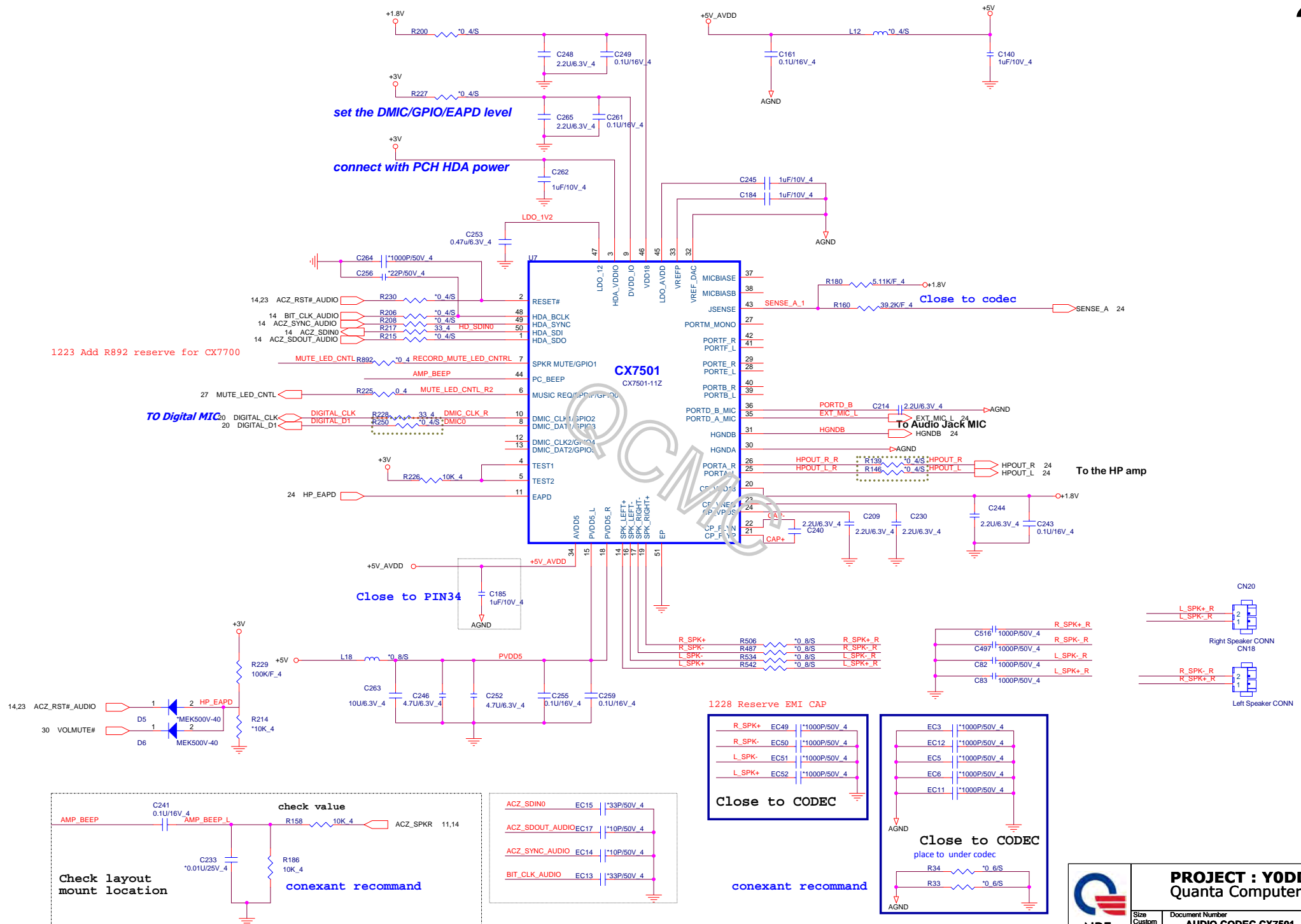


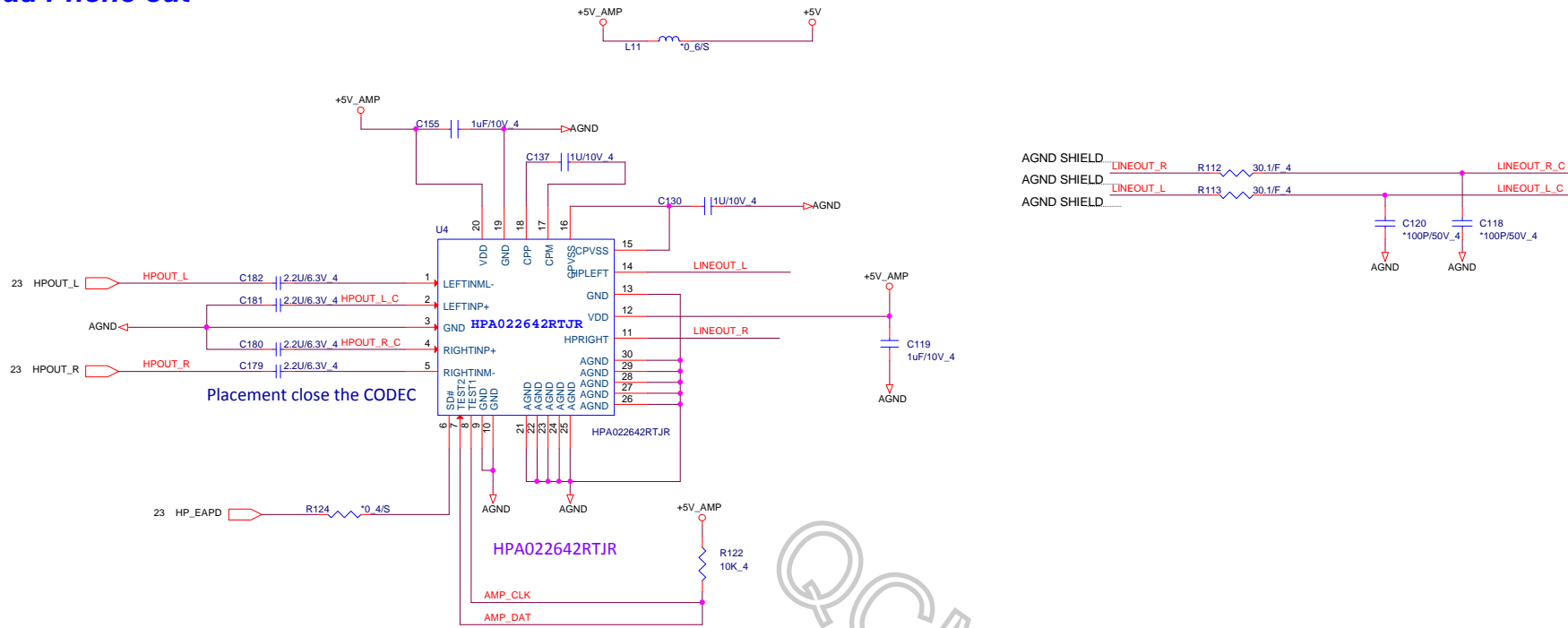
Mini Display



for intel recommend



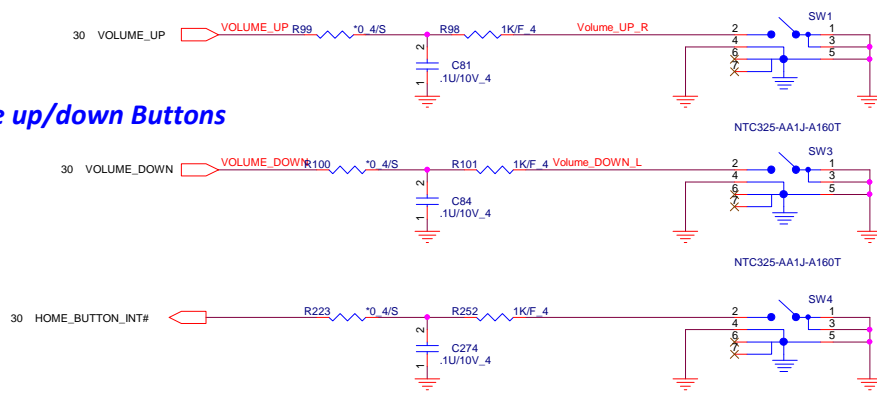




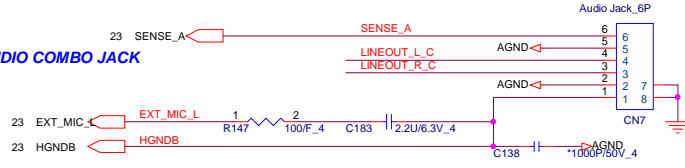
Audio combo JACK & Volume up/down Button

FAN

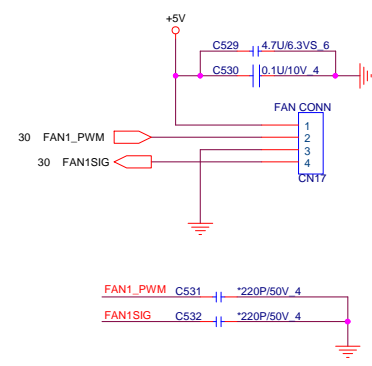
Volume up/down Buttons



AUDIO COMBO JACK



1203
Update footprint from 88266-0400-4p-1 to 88266-04x1-4p-1-sm

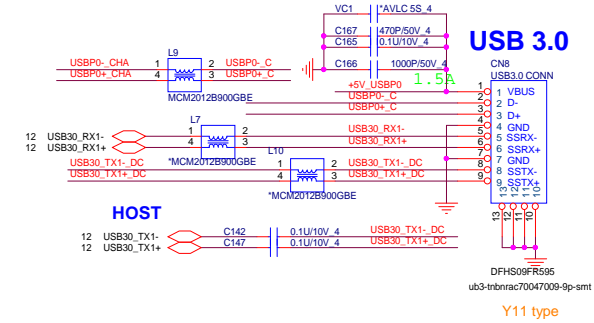
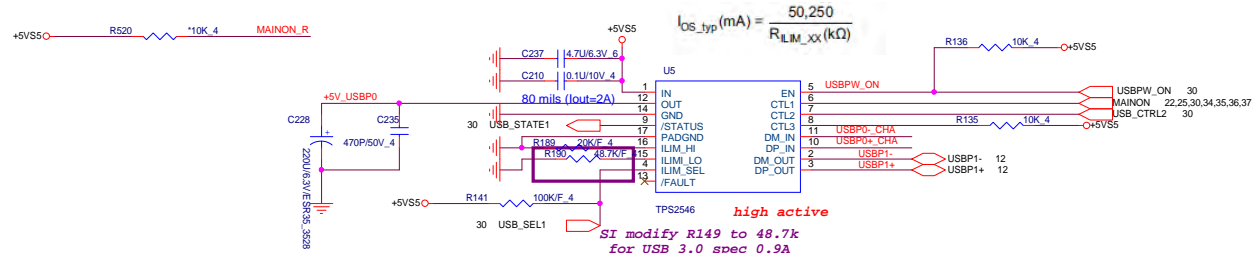


NB5

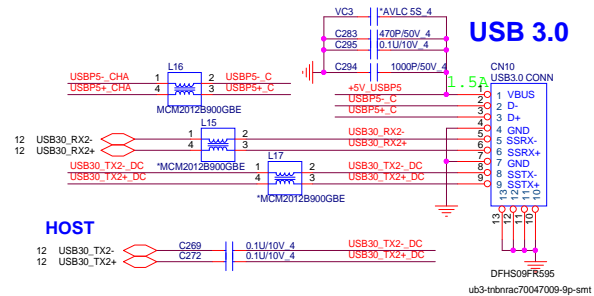
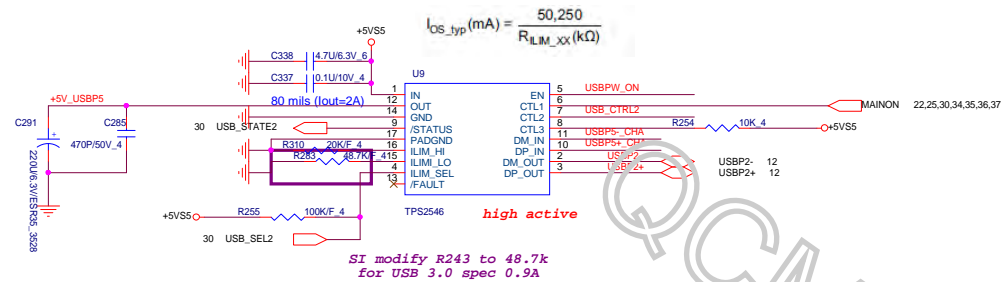
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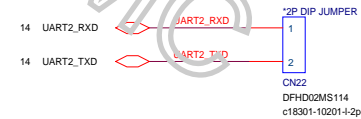
PV ADD R554/R555/R556 10k for USB 3.0 PU



1203
Update footprint from ub3-tbnbrac70047009-9p to ub3-tbnbrac70047009-9p-smt



UART



Left side USB 2.0/3.0 Combo

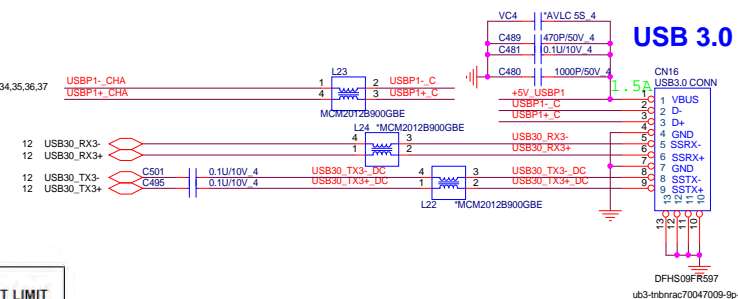
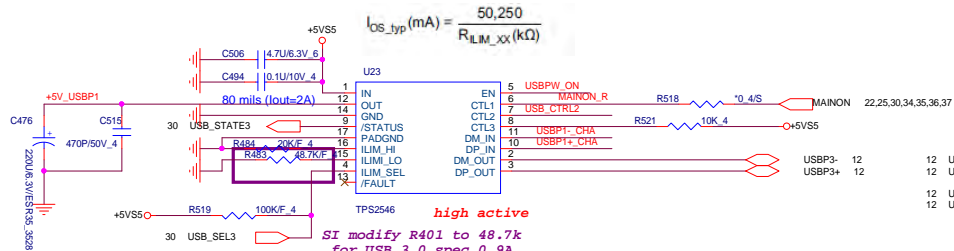


Table 3. Control Pin Settings Matched to System Power States

SYSTEM GLOBAL POWER STATE	TPS2546 CHARGING MODE	CTL1	CTL2	CTL3	ILIM_SEL	CURRENT LIMIT SETTING
S0	SDP1	1	1	0	1 or 0	ILIM_HI / ILIM_LO
S0	SDP2, no discharge to / from CDP	1	1	1	0	ILIM_LO
S0	CDP, load detection with ILIM_LO + 60mA thresholds or if a BC1.2 primary detection occurs	1	1	1	1	ILIM_HI
S4/S5	Auto mode, load detection with power wake thresholds	0	0	1	1	ILIM_HI
S3/S4/S5	Auto mode, no load detection	0	0	1	0	ILIM_HI
S3	Auto mode, keyboard/mouse wake up, load detection with ILIM_LO + 60 mA thresholds	0	1	1	1	ILIM_HI
S3	Auto mode, keyboard/mouse wake-up, no load detection	0	1	1	0	ILIM_HI
S3	SDP1, keyboard/mouse wake-up	0	1	0	1 or 0	ILIM_HI / ILIM_LO

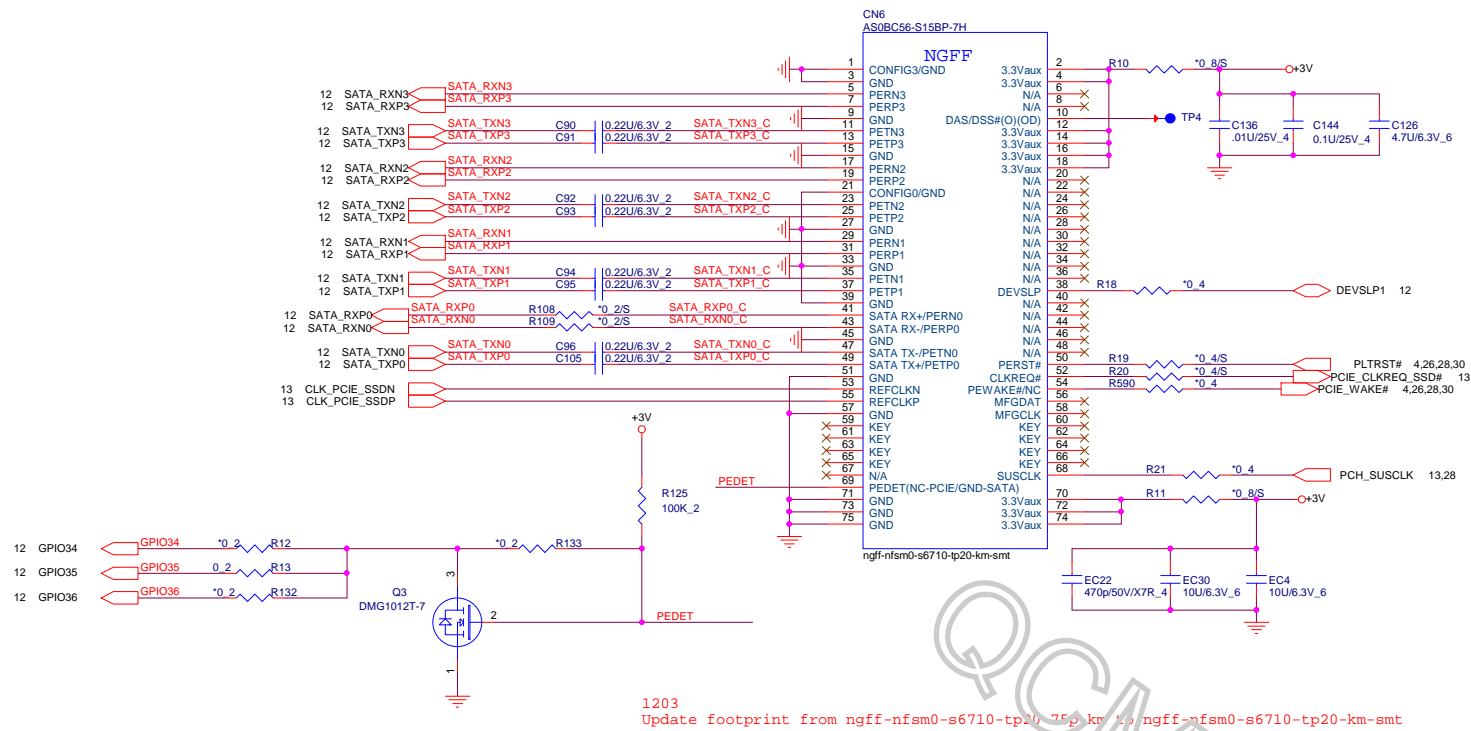
4,15,22,28,30,31,33,35,36,37
4,33,34,35,36,37,38,39,40
6,13,15,27,28,30,31,32,33

+5VSS
+5VSS
+3VPCU

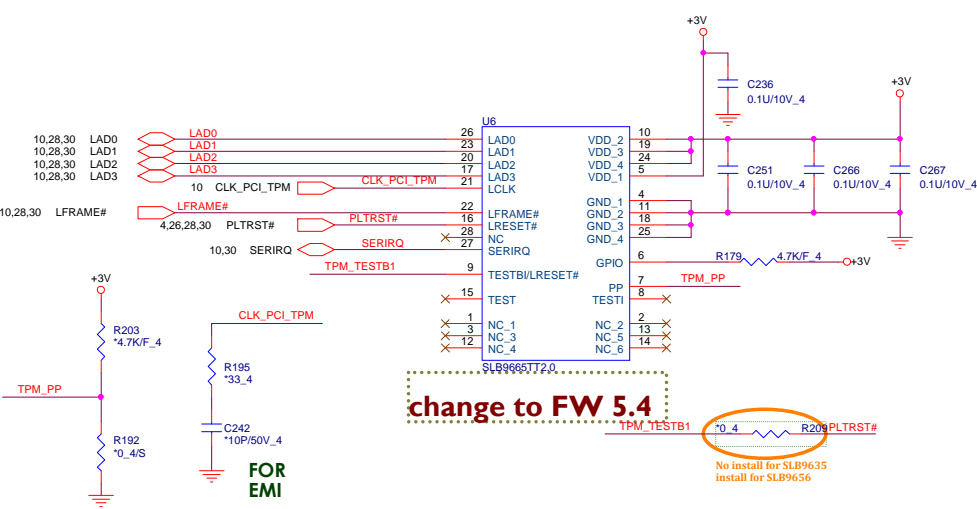


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Quanta Computer Inc.

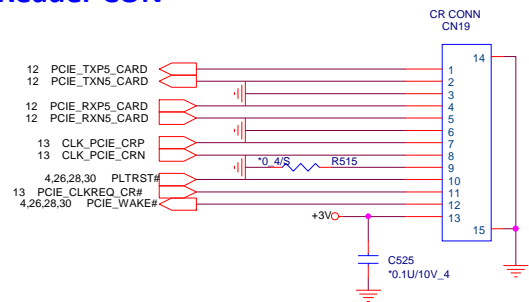
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TPM (2.0)



Card Reader CON

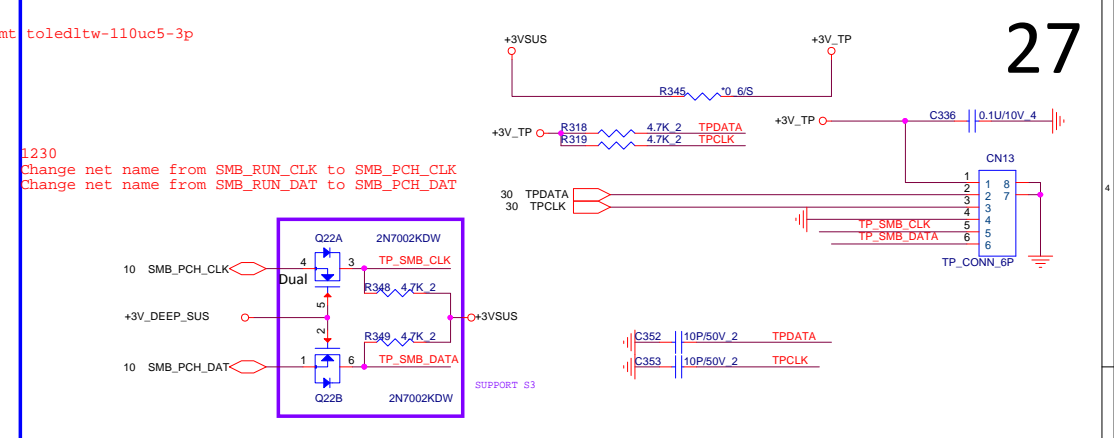
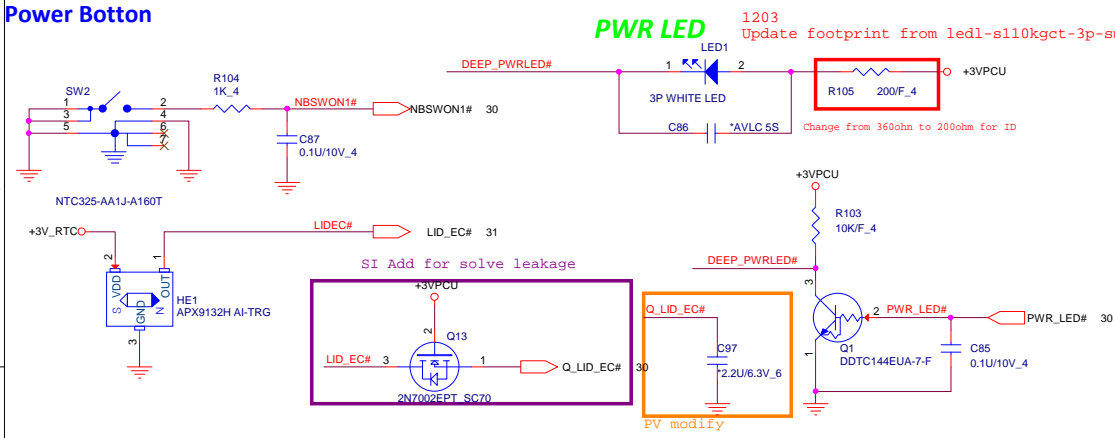


2,4,10,11,12,13,14,15,20,22,23,27,29,30,31,37,38 +3V
22,23,24,27,37 +5V
6,13,15,27,28,30,31,32,33 +3VPCU

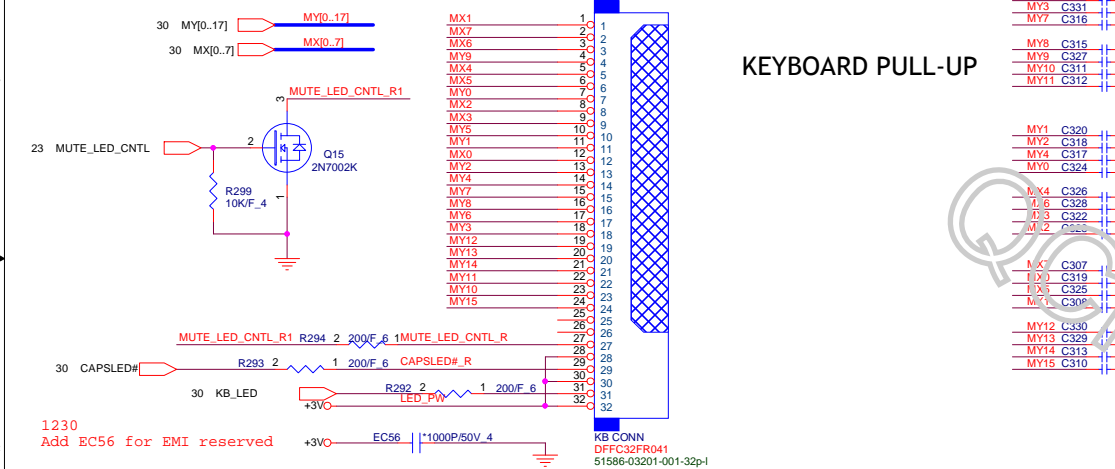
PROJECT : YODD
Quanta Computer Inc.

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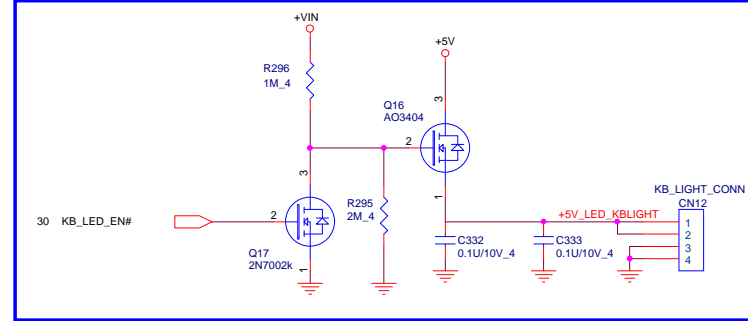
Power Button



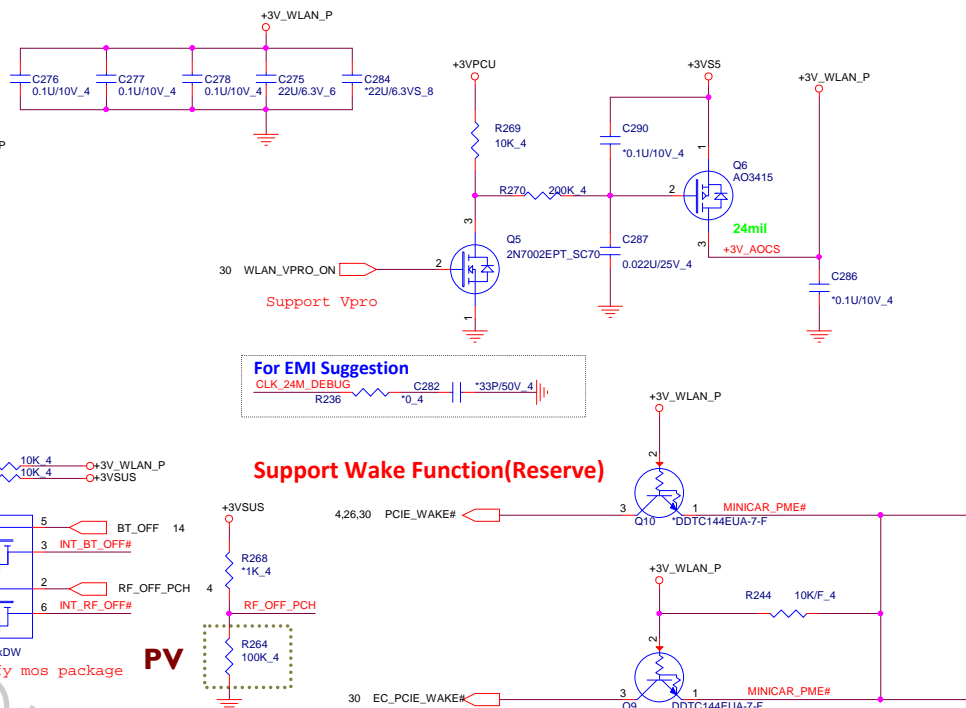
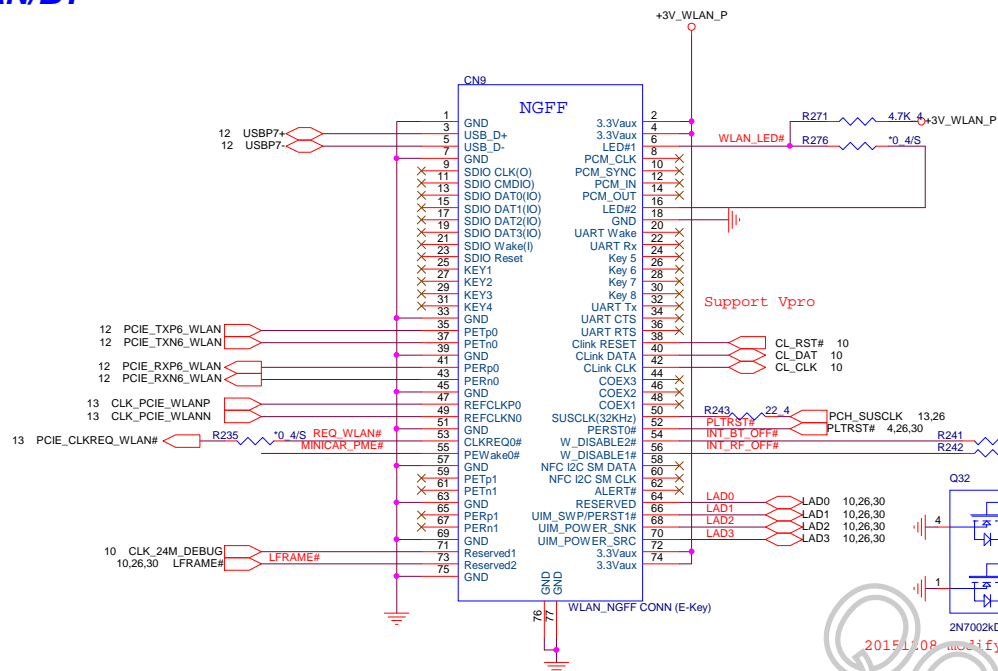
KEYBOARD Con.



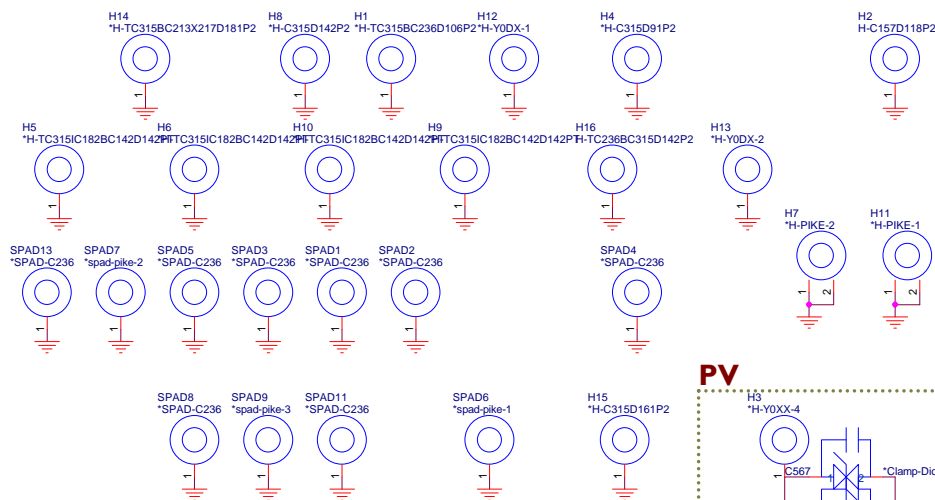
KB backlight



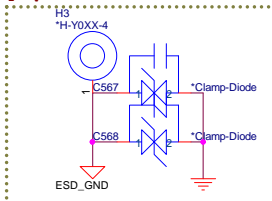
2,4,10,11,12,13,14,15,20,22,23,26,29,30,31,37,38 +3V
22,23,24,37 +5V
6,13,15,28,30,31,32,33 +3VPCU



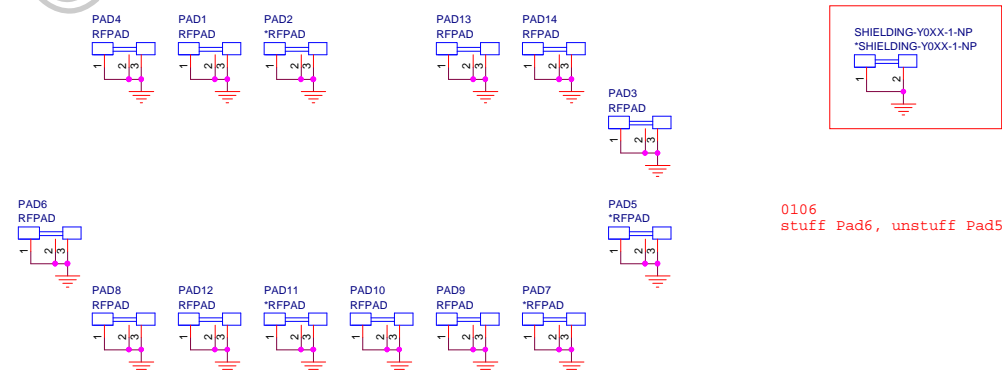
Hole

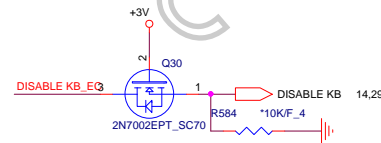
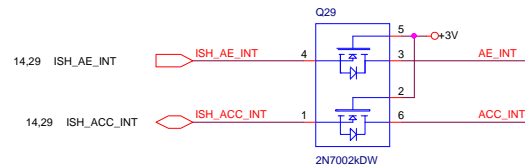
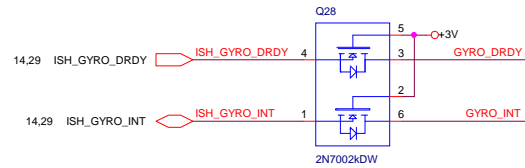
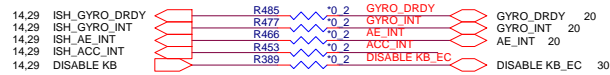


PV



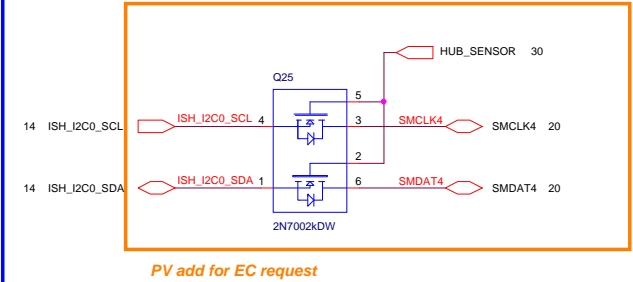
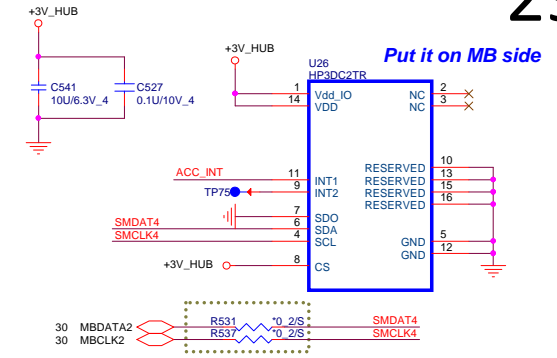
GND GUARD



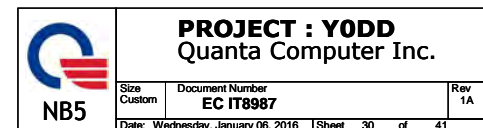


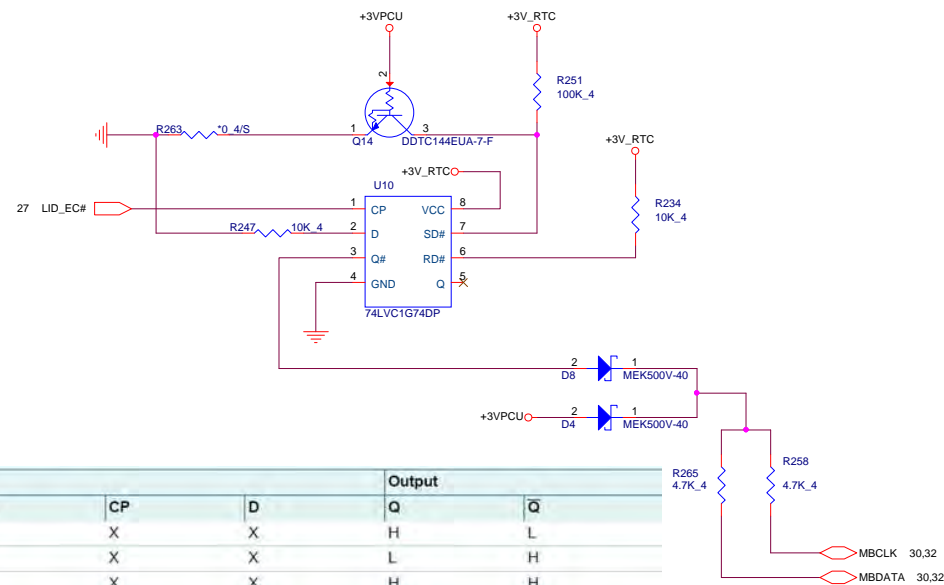
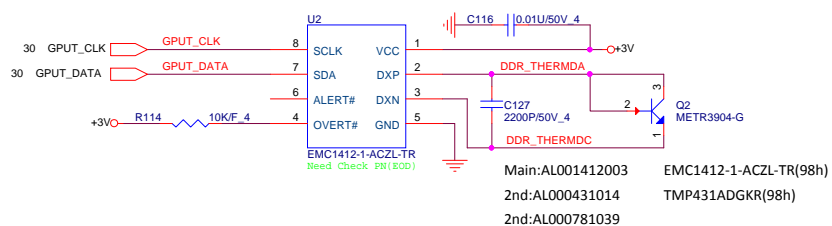
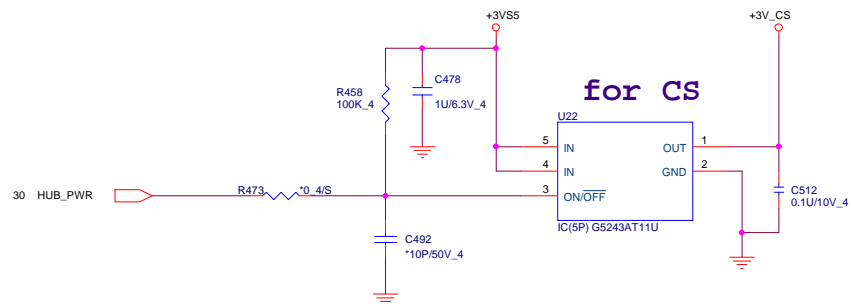
Accelerometer Sensor

29



1222
Del Q26/ R587/ R588 for OLED reserve



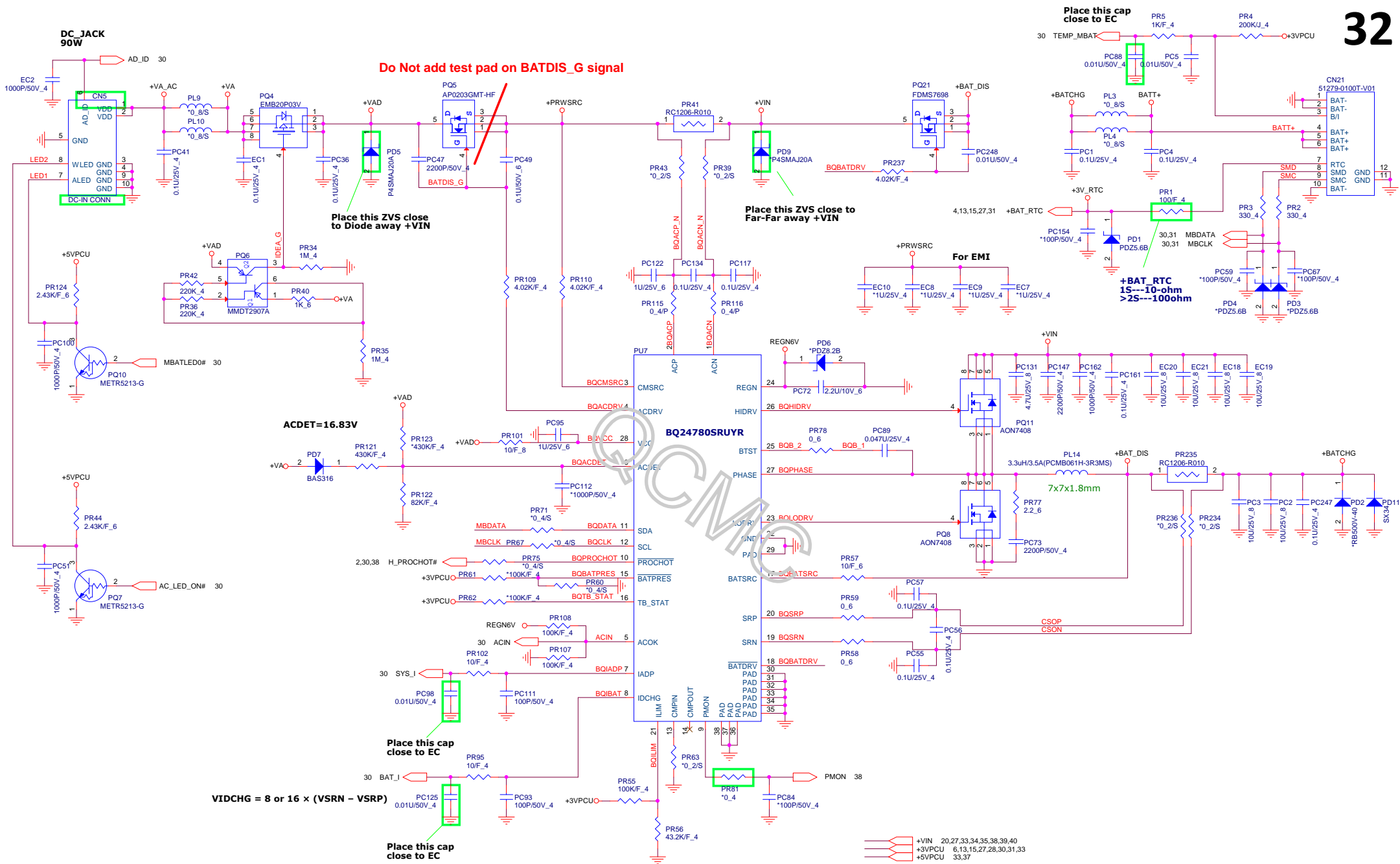


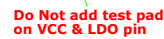
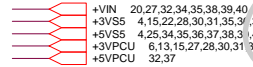
Input				Output	
SD	RD	CP	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care.

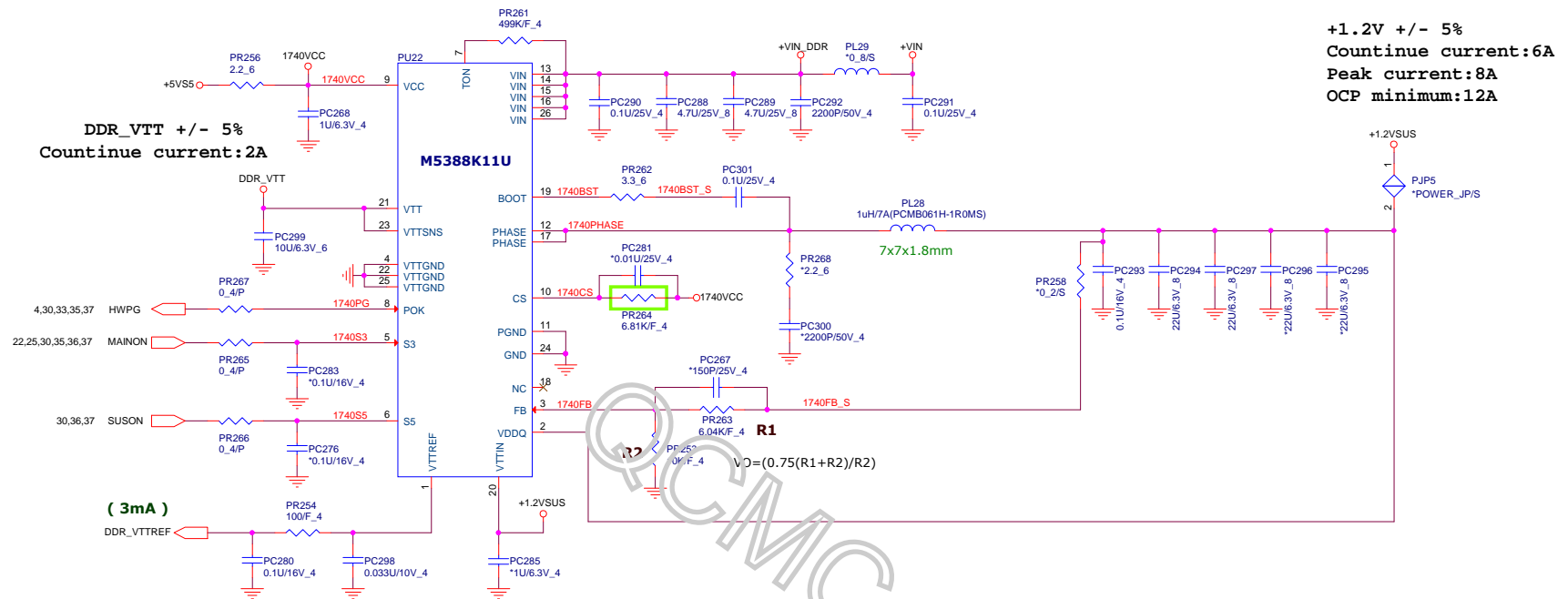
Input				Output	
SD	RD	CP	D	Q _{n+1}	Q̄ _{n+1}
H	H	↑	L	L	H
H	H	↑	H	H	L

[1] H = HIGH voltage level;
L = LOW voltage level;
↑ = LOW-to-HIGH CP transition;
Q_{n+1} = state after the next LOW-to-HIGH CP transition.



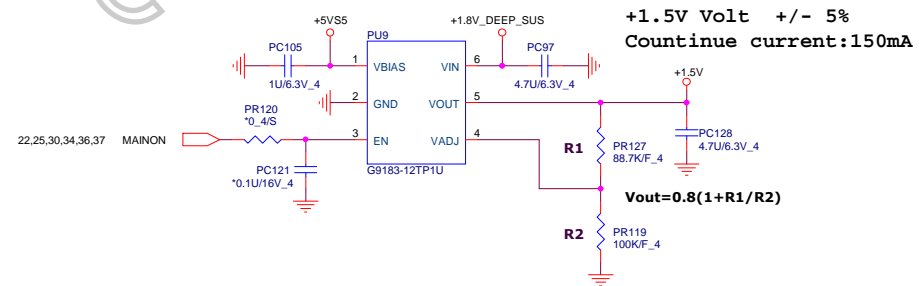
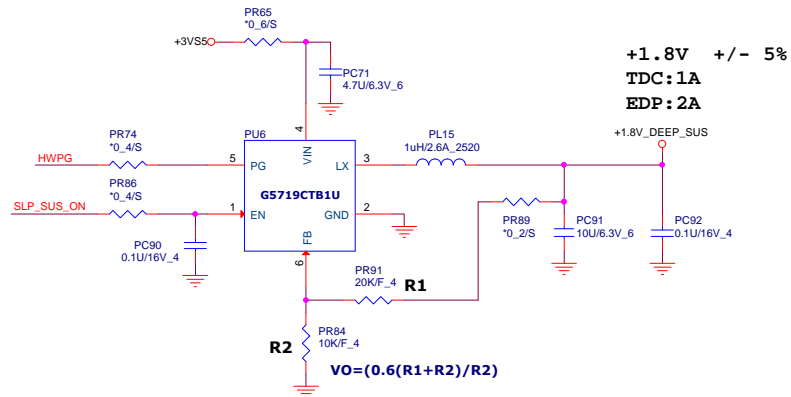
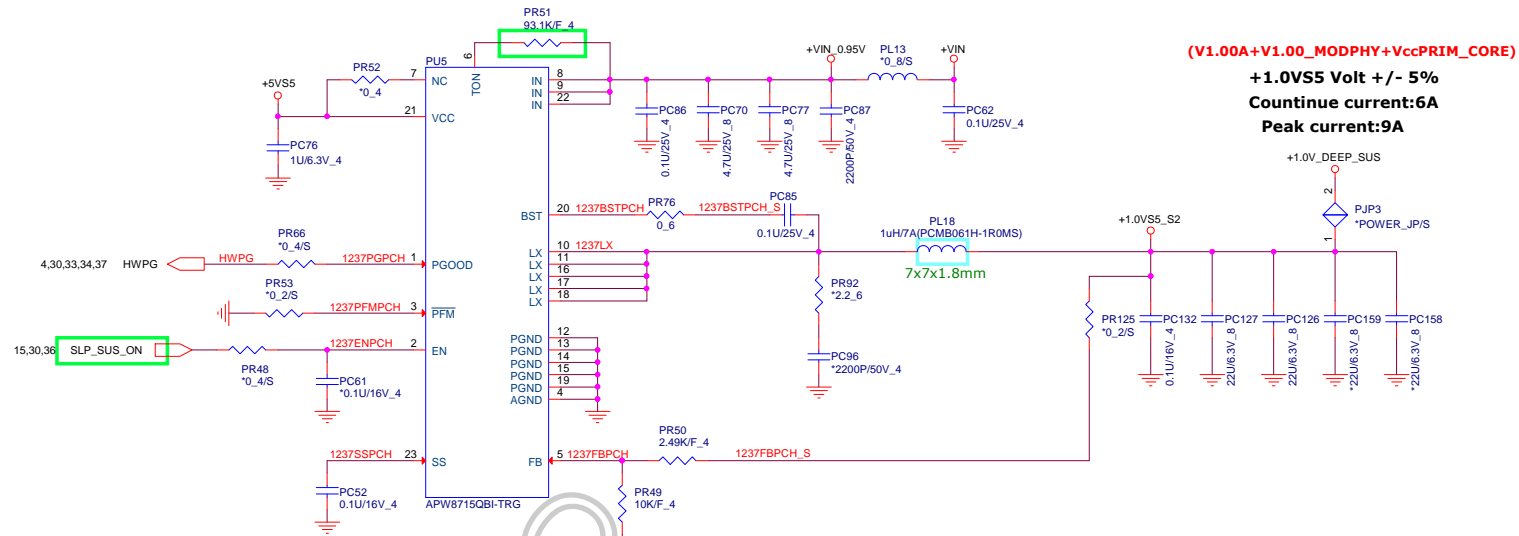


USB Charge Support	Ra	Rb
No support	Stuff	NA
Support	NA	Stuff



	S3	S5	+1.2VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

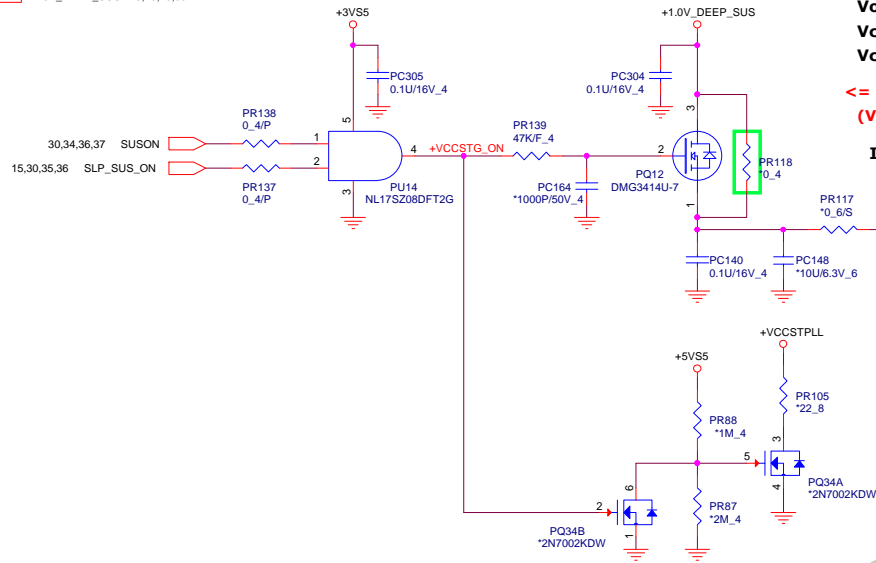
+VIN 20,27,32,33,34,38,39,40
 +3VS5 4,15,22,28,30,31,33,36,37
 +5VS5 4,25,33,34,36,37,38,39,40
 +1.0V_DEEP_SUS 9,13,15,36
 +1.8V_DEEP_SUS 9,15,37



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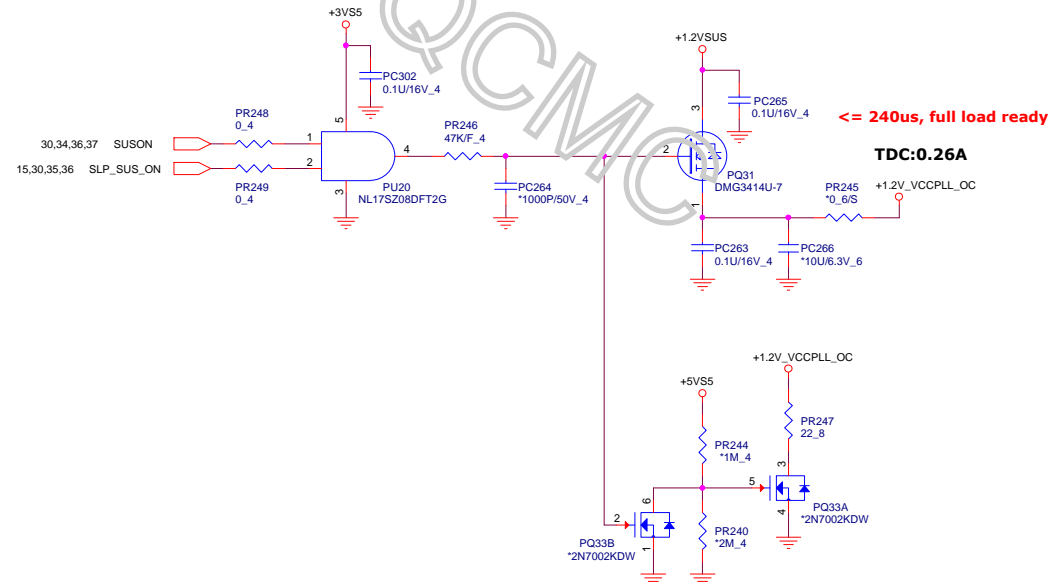
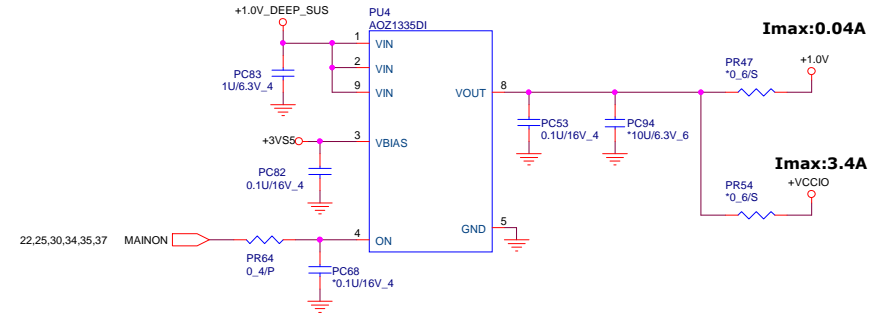
+1.0V 2,4,6,30
 +3VS5 4,15,22,28,30,31,33,35,37
 +5VS5 4,25,33,34,35,37,38,39,40
 +VCCIO 2,6,16
 +VCCSTPLL 2,5,6,9,38
 +1.0V_DEEP_SUS 9,13,15,35

**Volume Segment****Vcc_ST: 0.12A****Vcc_PLL: 0.12A**

<= 10ms, full load ready
 (Vcc_ST+Vcc_PLL)

Imax:0.24A**Volume Segment****Vcc_STG: 0.04A****Vcc_IO: 3.4A**

<= 10ms full load ready

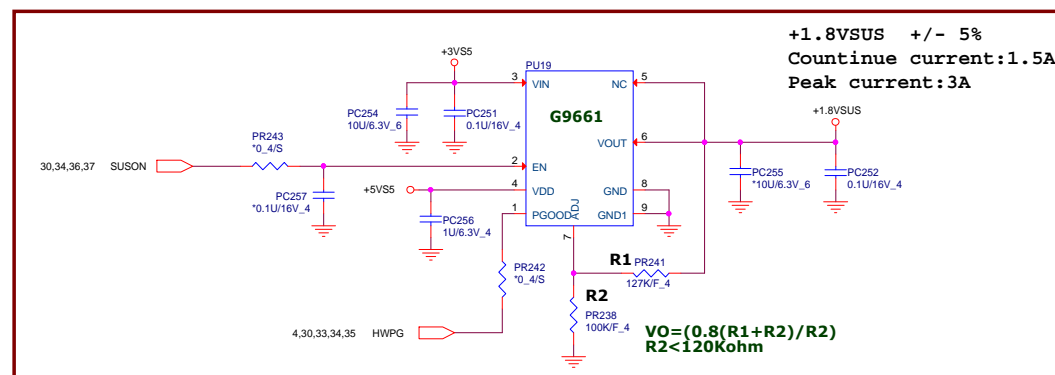
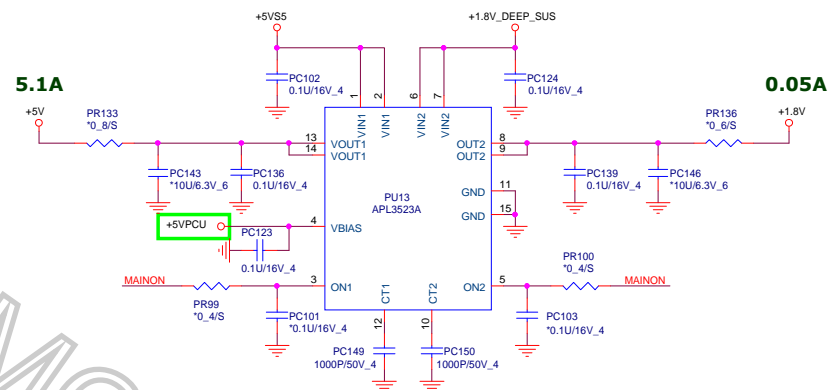
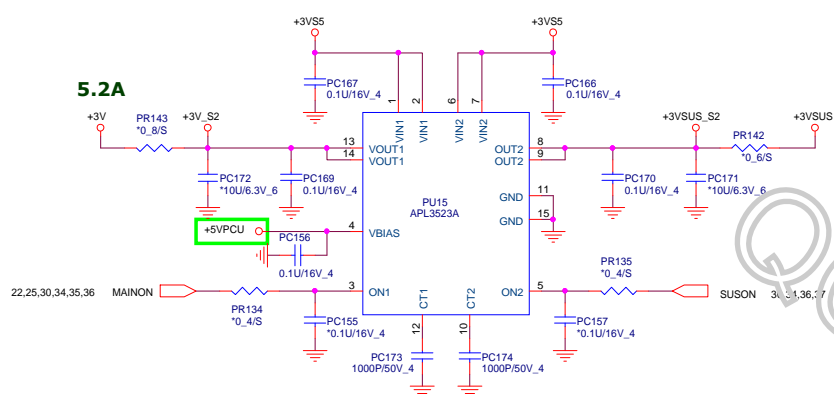
Imax:0.04A**Imax:3.4A**

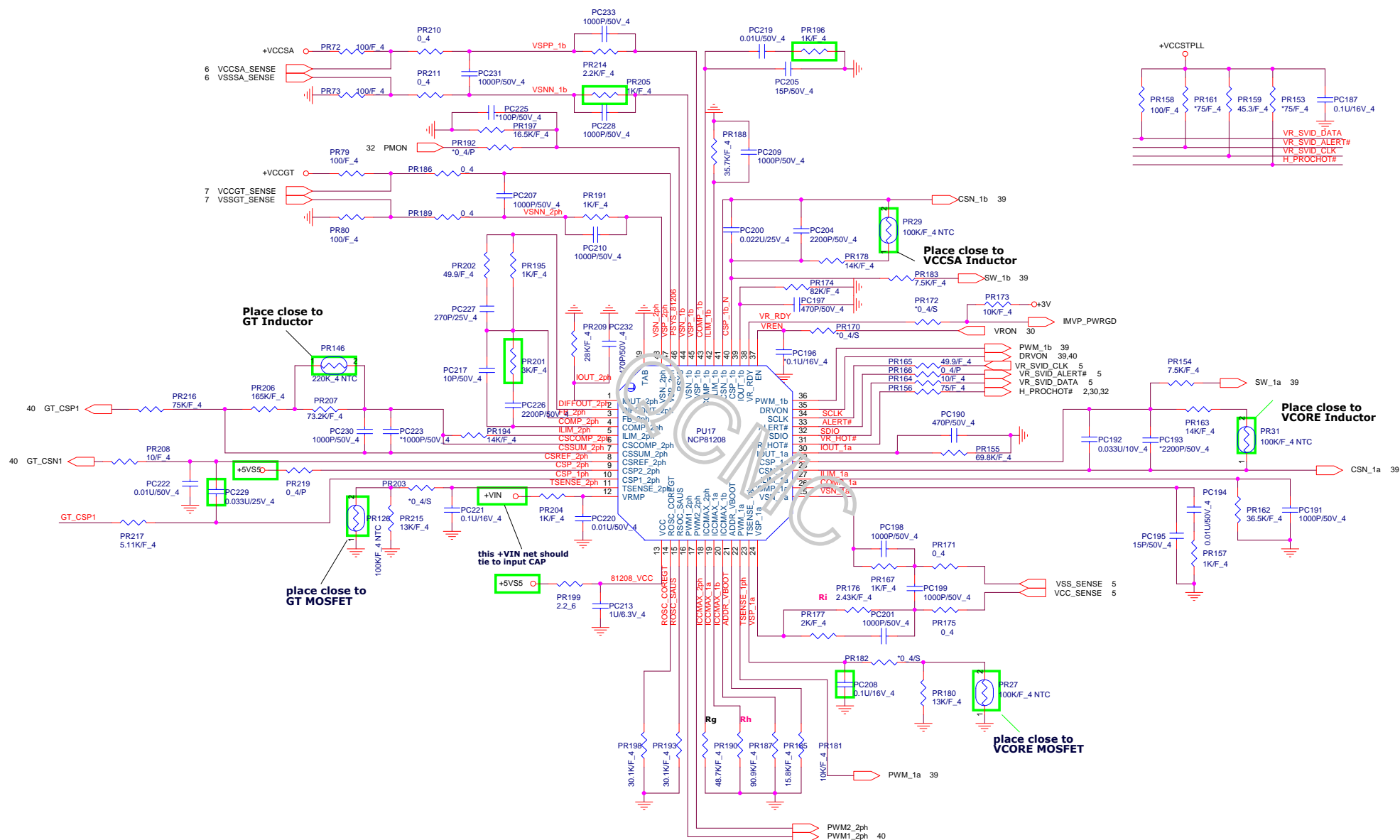
<= 240us, full load ready

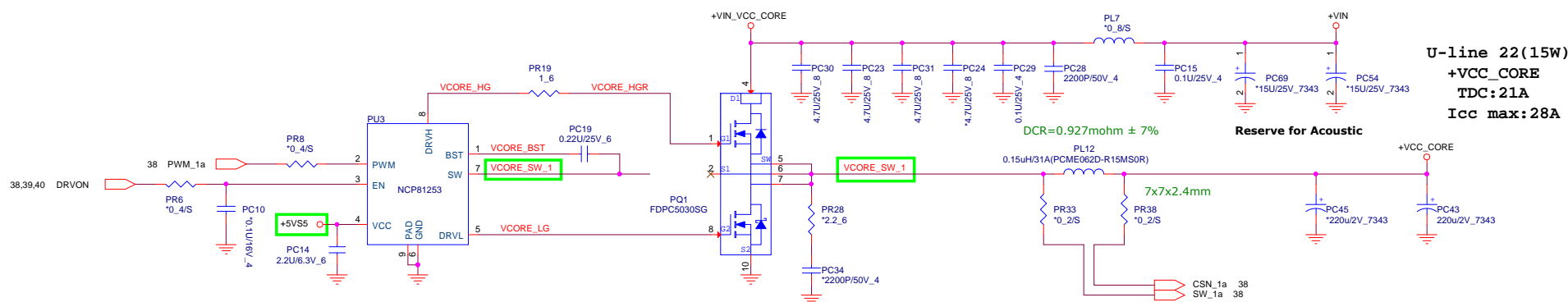
TDC:0.26A

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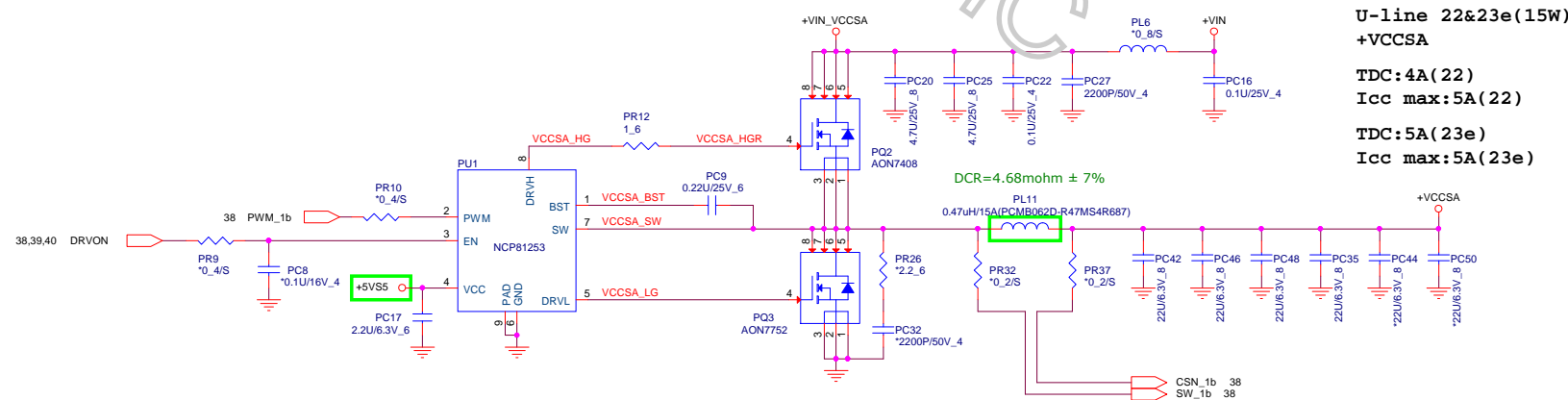
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Custom	+1.0V/+VCCSTPLL	1A
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VCCSA



+VIN 20,27,32,33,34,35,38,39
 +VCCGT 7,38
 +VIN_VCC_CORE
 +5VPCU 32,33,37
 +5V 22,23,24,27,37

